

Cottonwood Schematic Broadwell-ULT

2014-06-09

REV : A00

DY : None Installed

Eletro-X

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wai Rd., Neihu,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size

A3

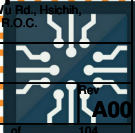
Document Number

Cottonwood

Date: Tuesday, June 17, 2014

Sheet 1

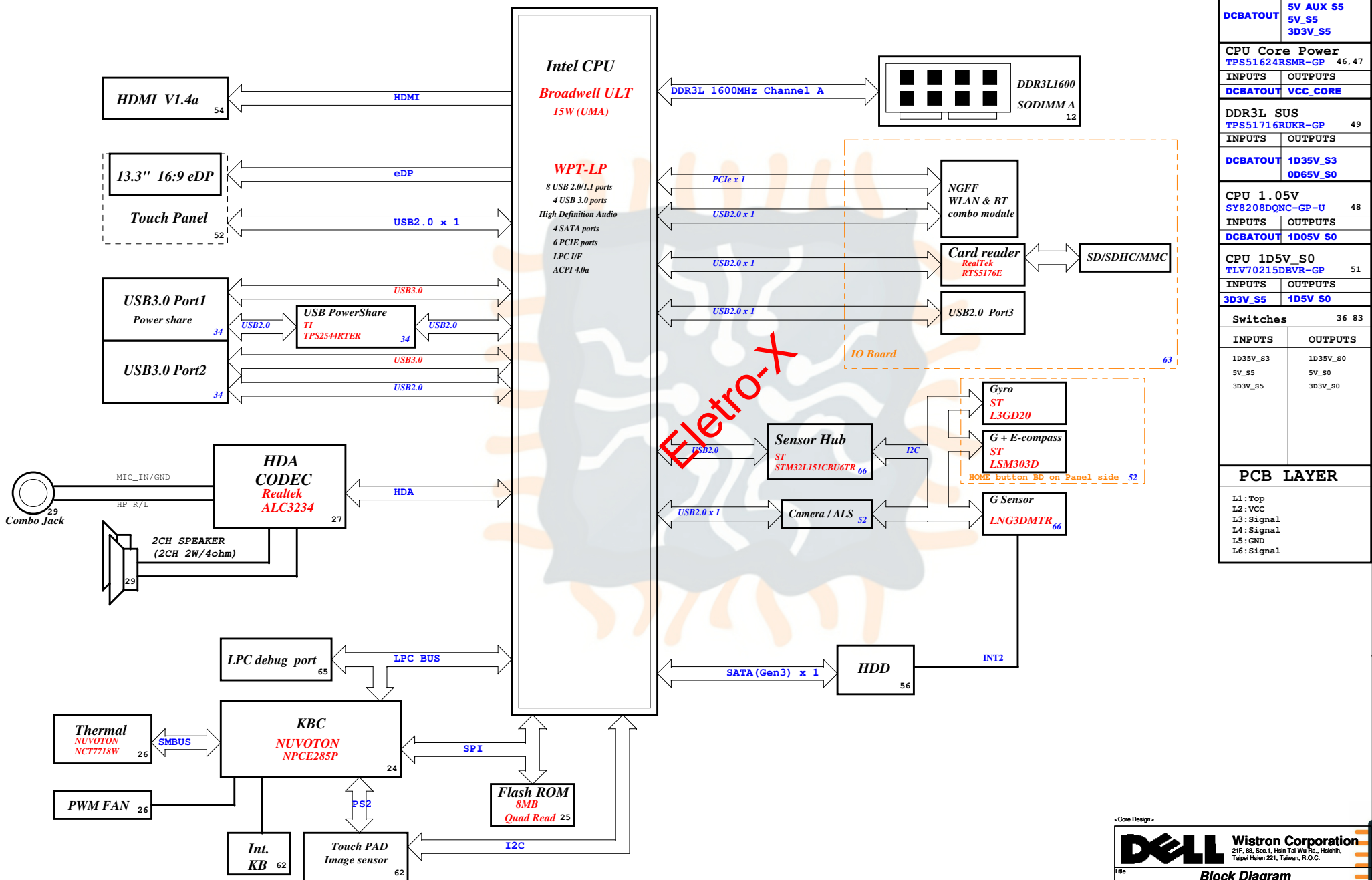
of 103



ELETRO-X

Project code:4PD01V010001
PCB P/N: 13321
Revision: A00

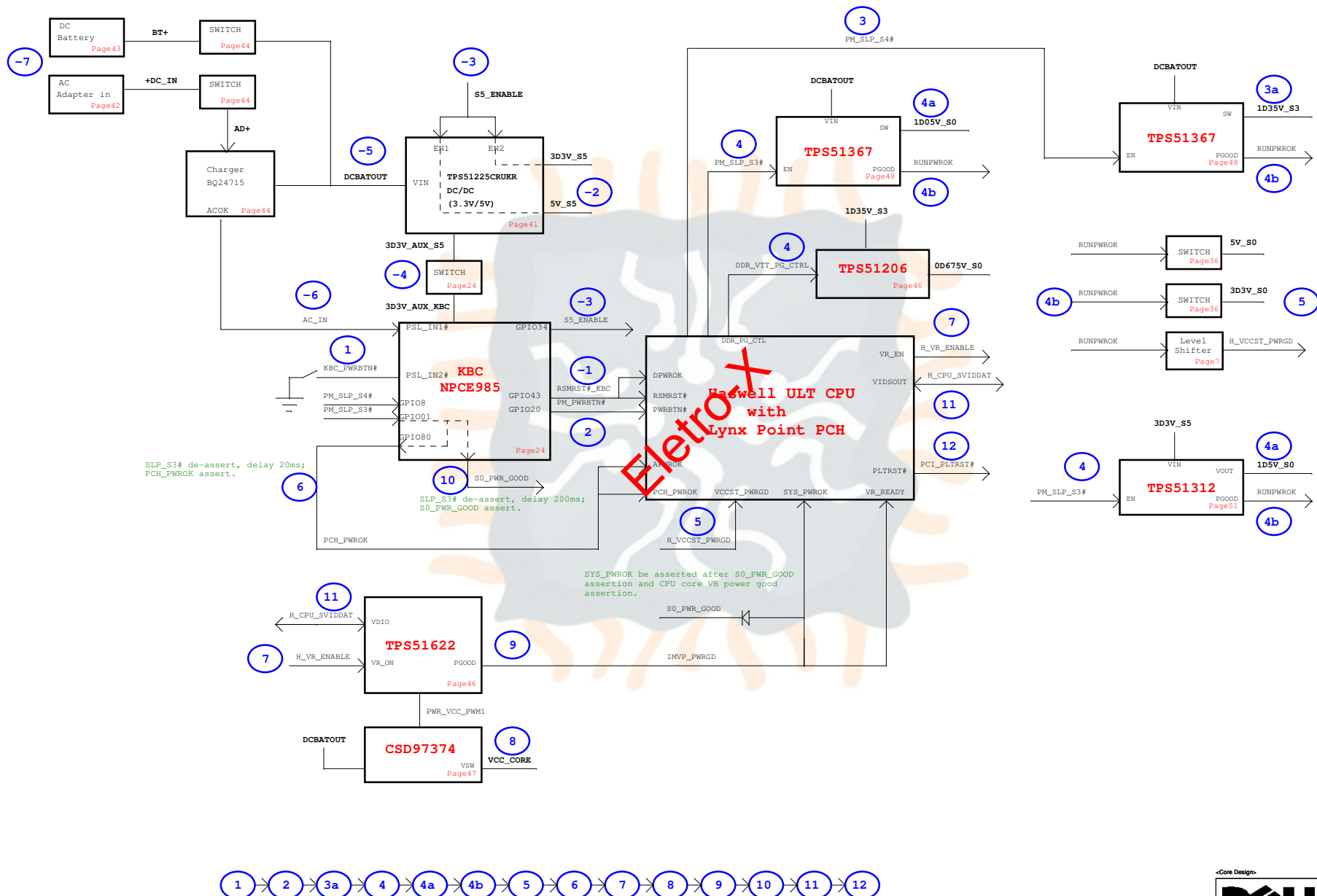
Cottonwood Block Diagram



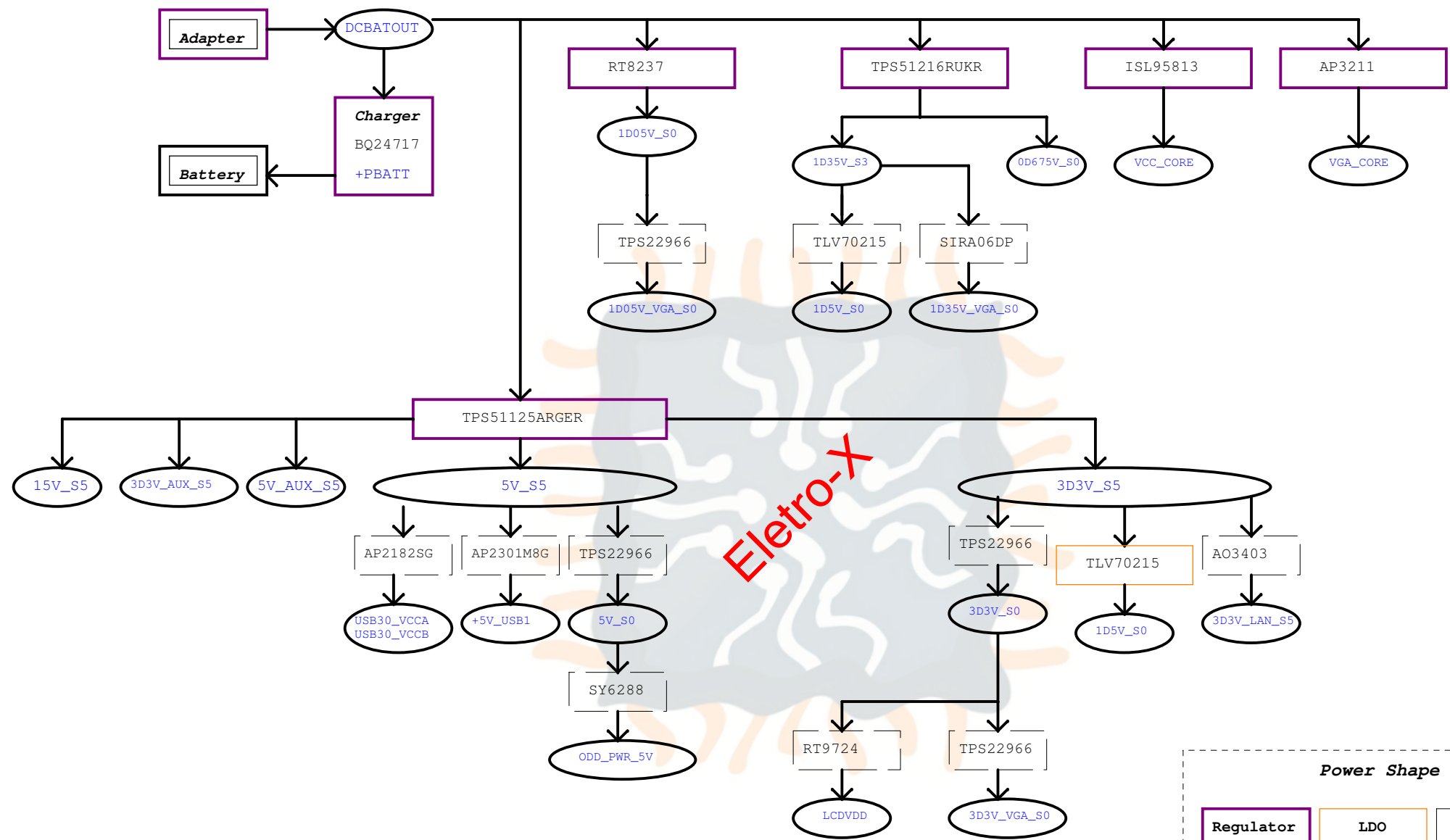
CHARGER	
BQ24770UYR-GP	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
TPS51624RSMR-GP	46, 47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
SY8208DQNC-GP-U	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1D5V_S0	
TLV70215DBVR-GP	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
36	83
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
PCB LAYER	
L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Signal	



Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



ELECTRO-2



EleTRO-X

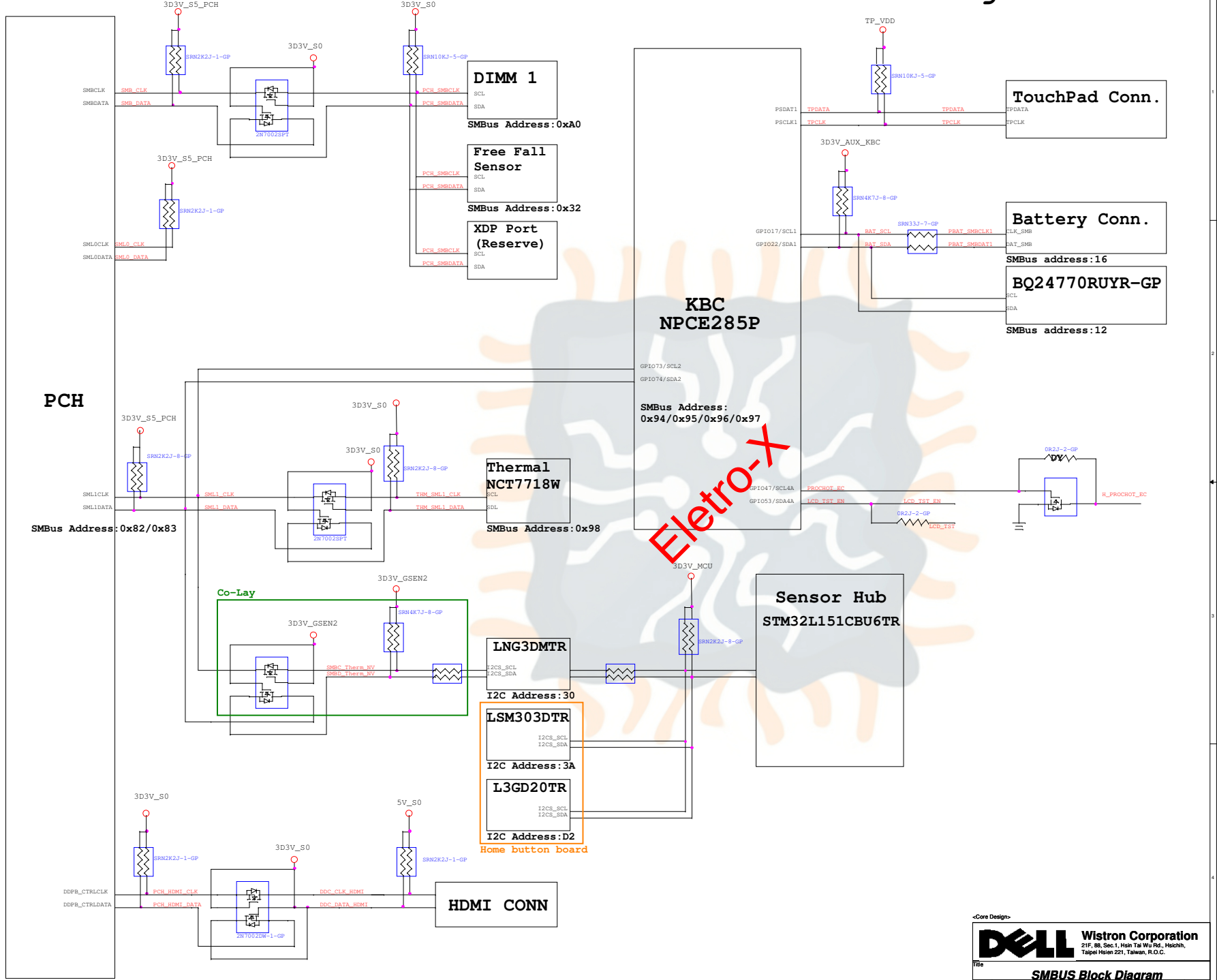
Power Shape

Regulator	LDO	Switch
-----------	-----	--------

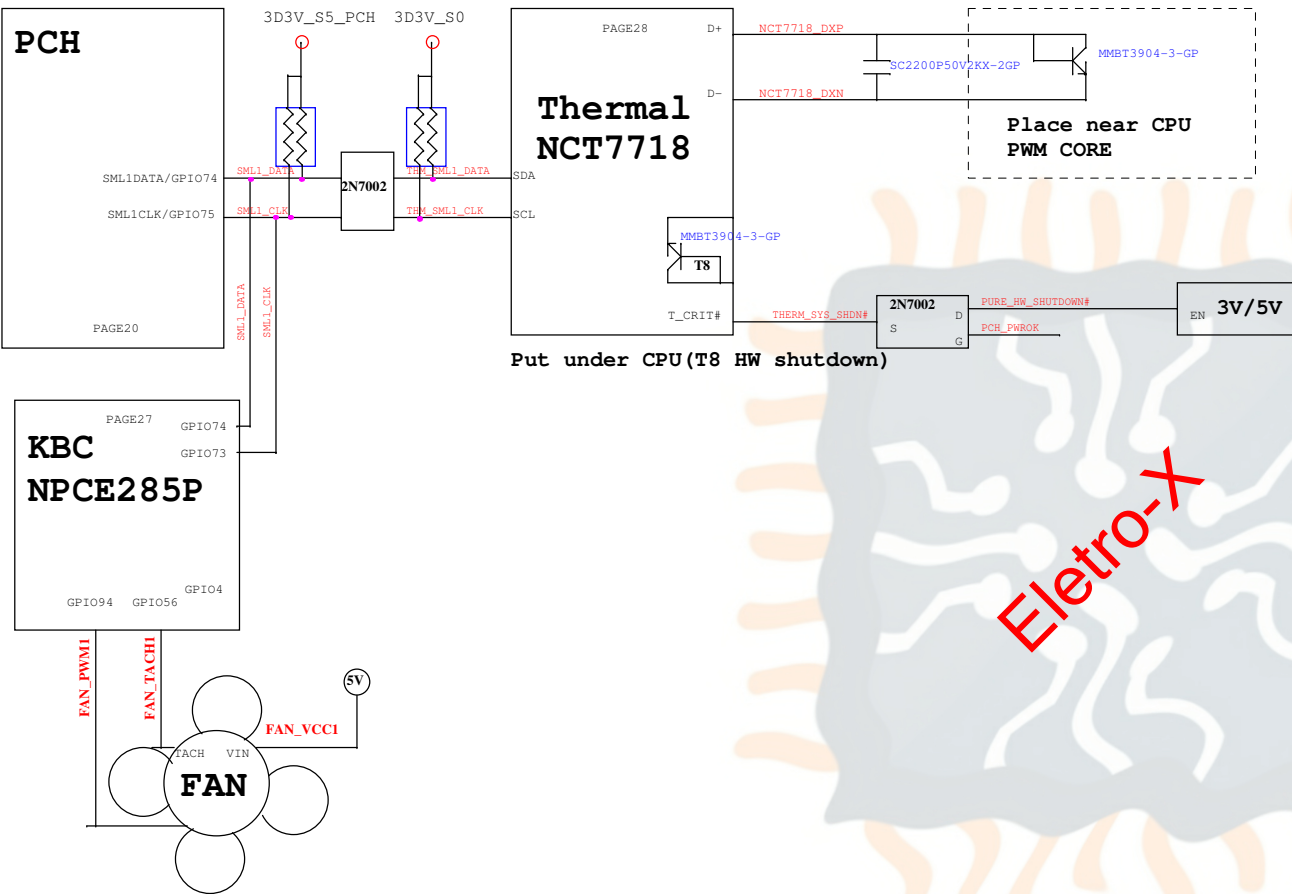
EleTRO-X

PCH SMBus Block Diagram

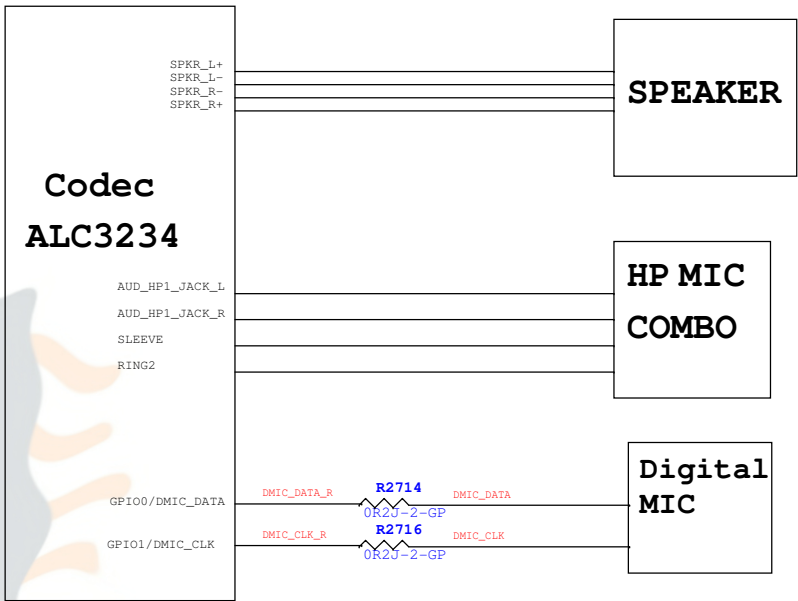
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



ELECTRO-2

SSID = CPU

Layout Note:

Impedance control: 50 ohm

[24,44,46] H_PROCHOT# <<<>>>

[12] DDR_PG_CTRL <<<>>>

Layout Note:

Design Guideline:

SM_RCOMP keep routing length less than 500 mils.

Layout Note:

Place close to DIMM

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Title

CPU (THERMAL/MISC/PM)

Size
A4

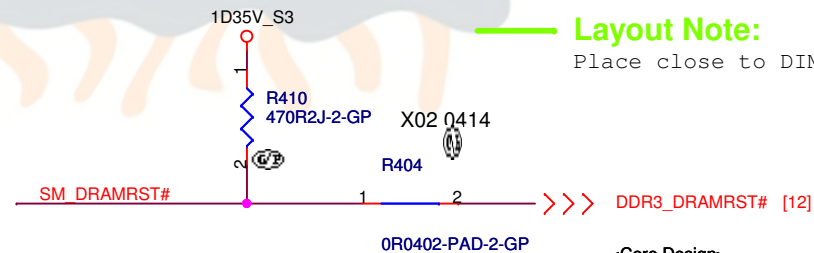
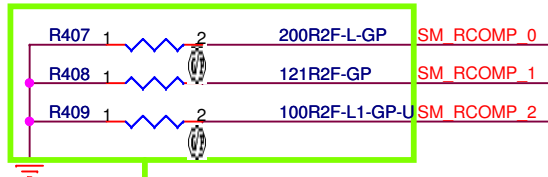
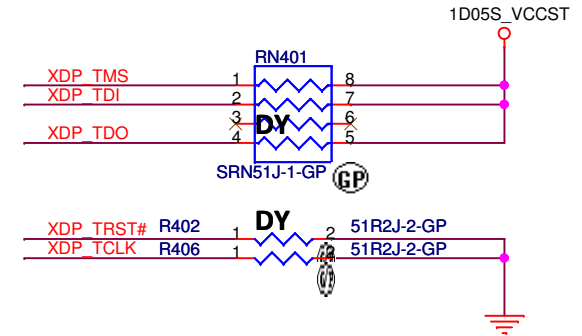
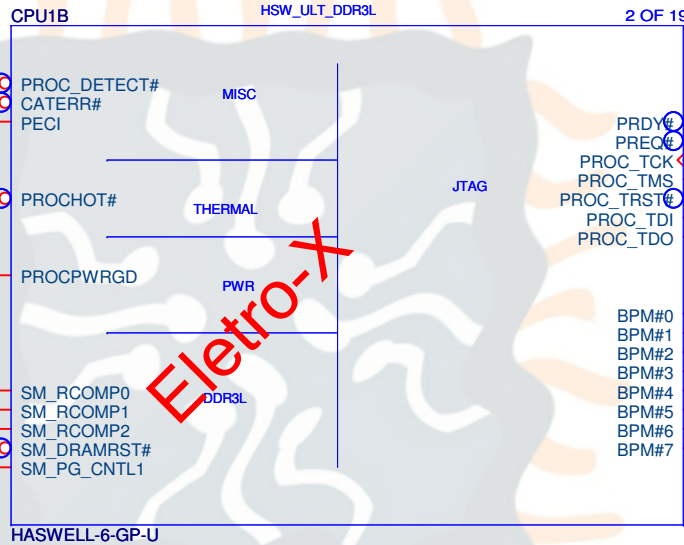
Document Number

Cottonwood

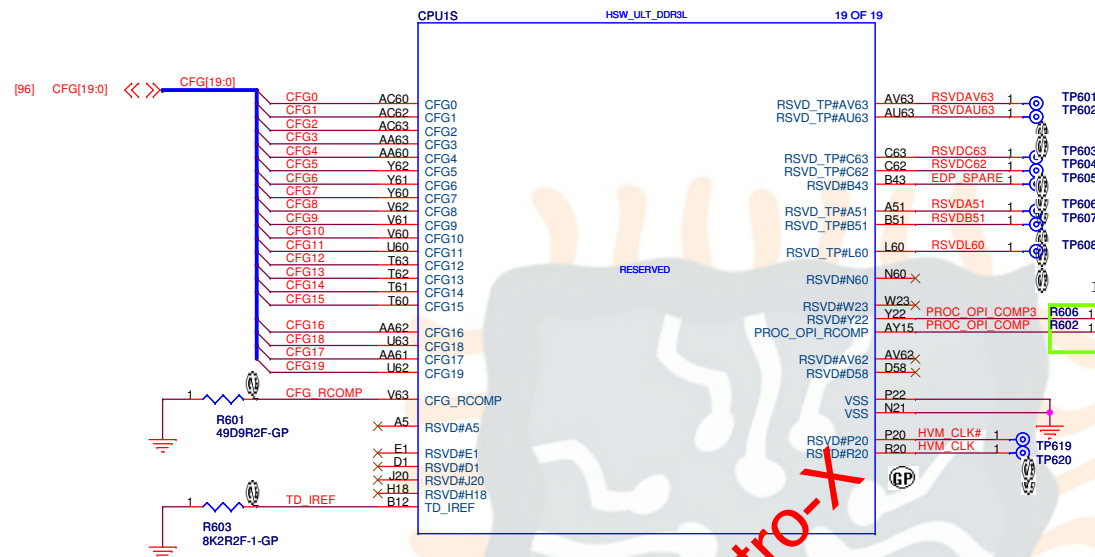
Date: Tuesday, June 17, 2014

Sheet 4 of 104

ELECTRO-2



SSID = CPU



7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

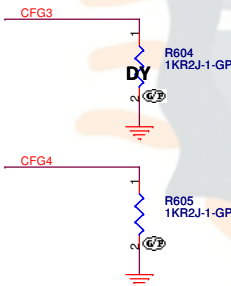
Intel Recommend

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none">• CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• CFG[3]: MSR Privacy Bit Feature<ul style="list-style-type: none">— 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting— 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden• CFG[4]: eDP enable<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lanes.	I/O GTL

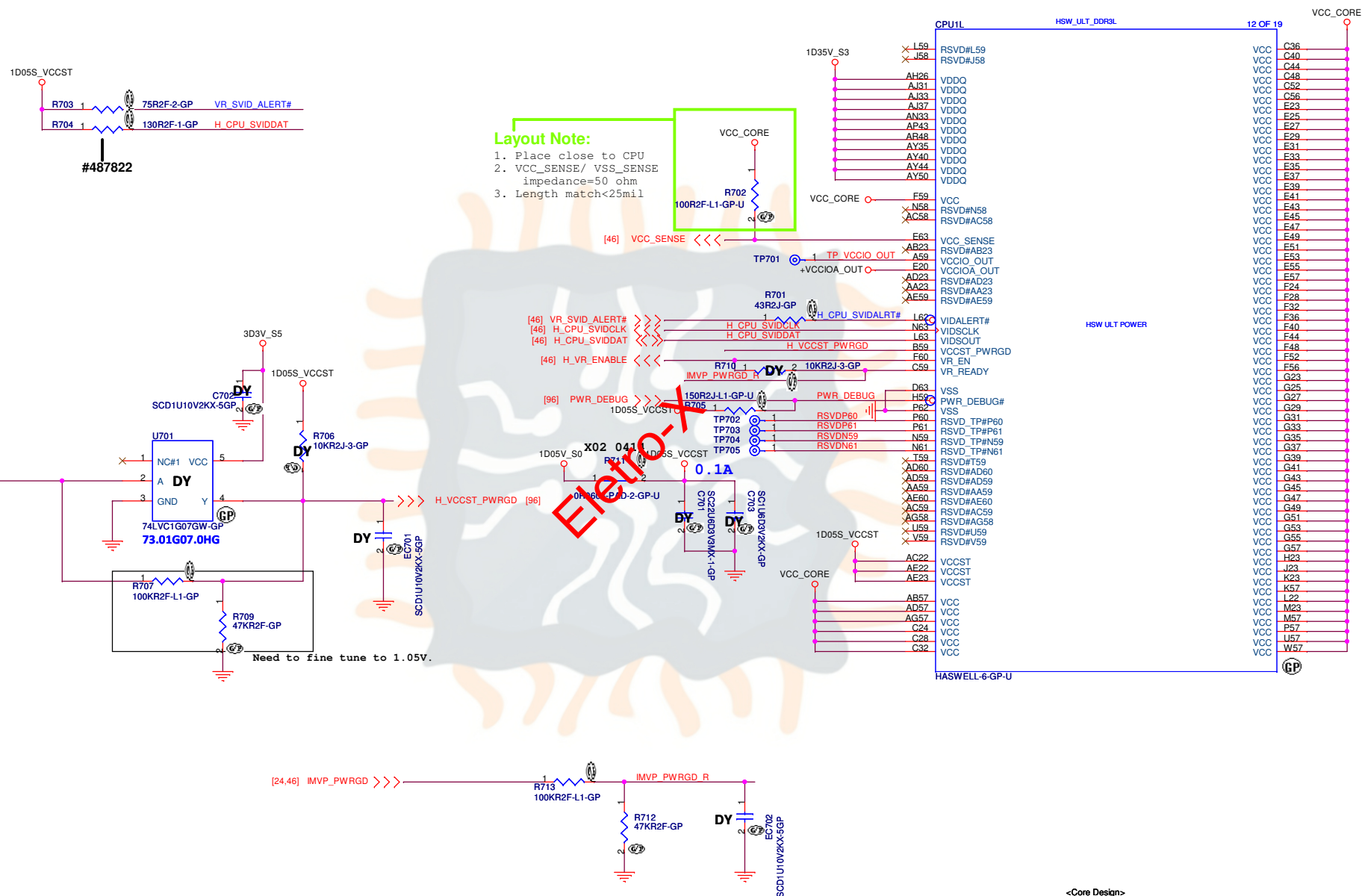


PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX_ENABLED BIT IN DEBUG_INTERFACE_MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>


SSID = CPU



<Core Design>



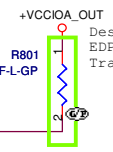
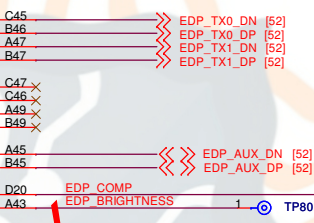
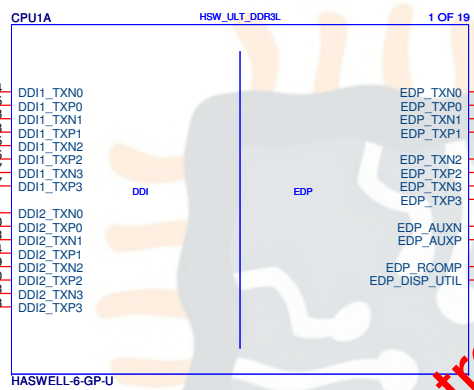
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Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU (VCC CORE)		
Size A3	Document Number	Cottonwood		
Date: Tuesday, June 17, 2014	Sheet	7	of 10	

ELECTRO-2

SSID = CPU

HDMI



Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Eletron-X

ELETRON-X

<Core Design>

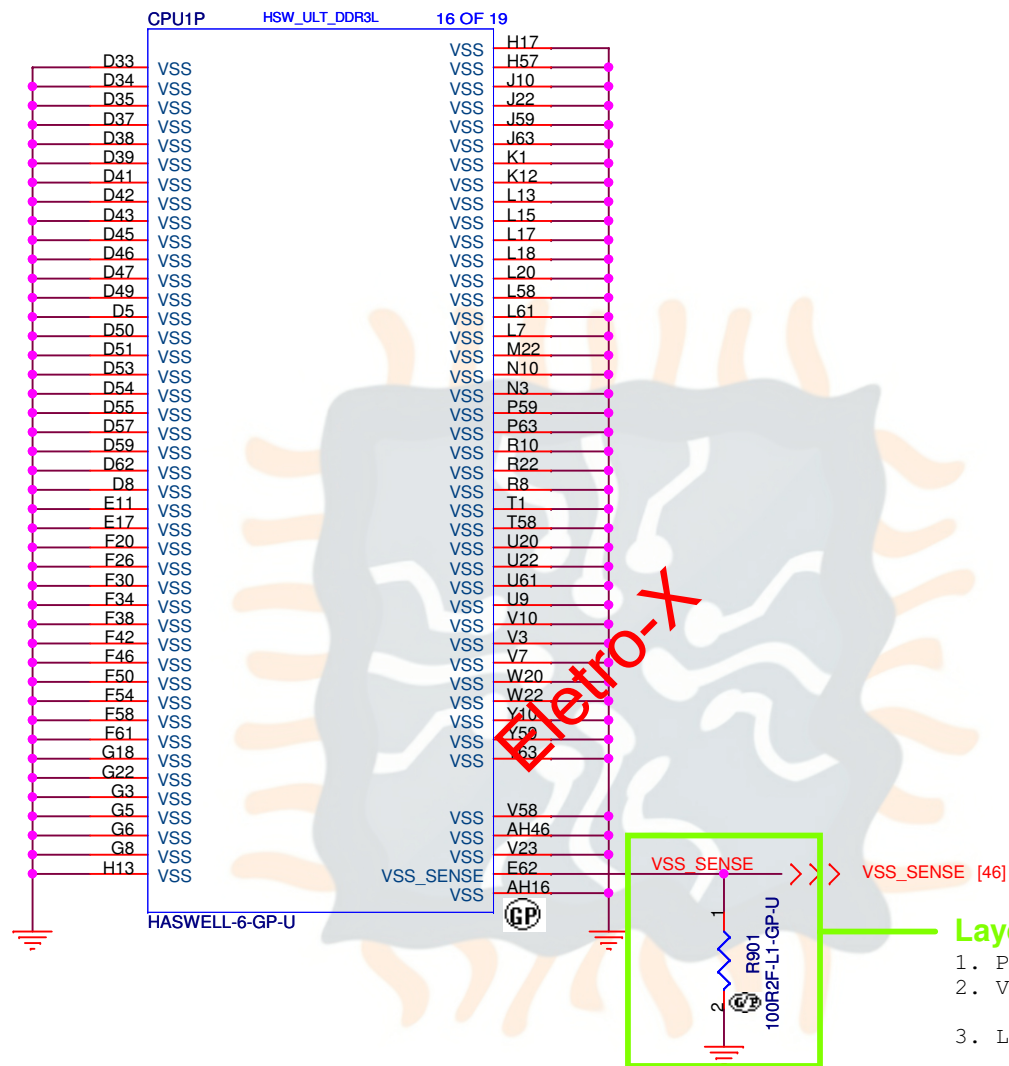
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

CPU (DDI/EDP)

Size A3 Document Number **Cottonwood** Rev A00

Date: Tuesday, June 17, 2014 Sheet 8 of 104

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title

CPU (VSS)

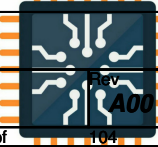
Size
A4

Document Number

Cottonwood

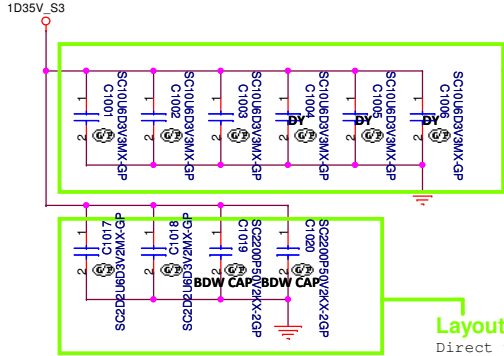
Date: Tuesday, June 17, 2014

Sheet 9 of 104



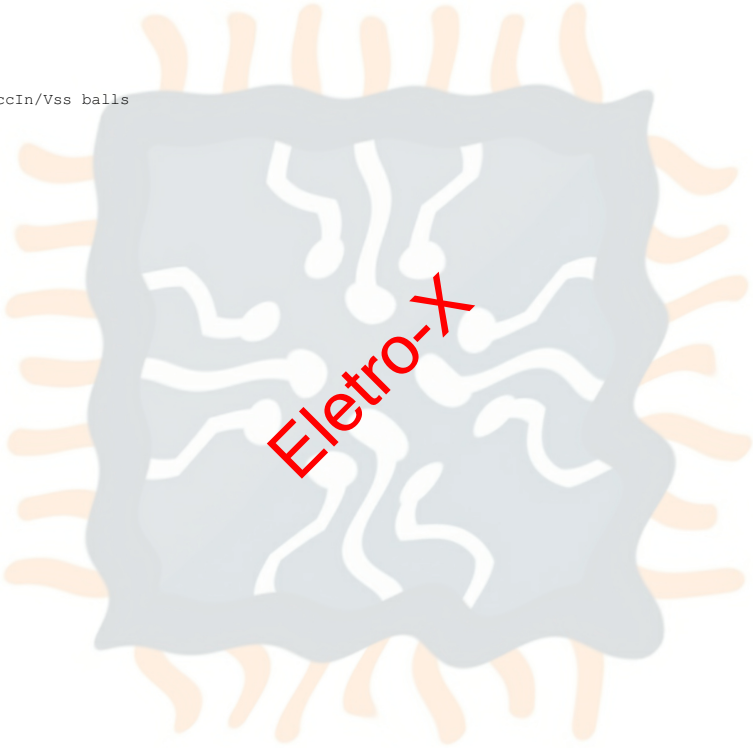
ECE+R0-2

SSID = CPU




Layout Note:
As close to CPU as possible

Layout Note:
Direct tie to CPU VccIn/Vss balls



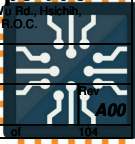
ELETRO-X

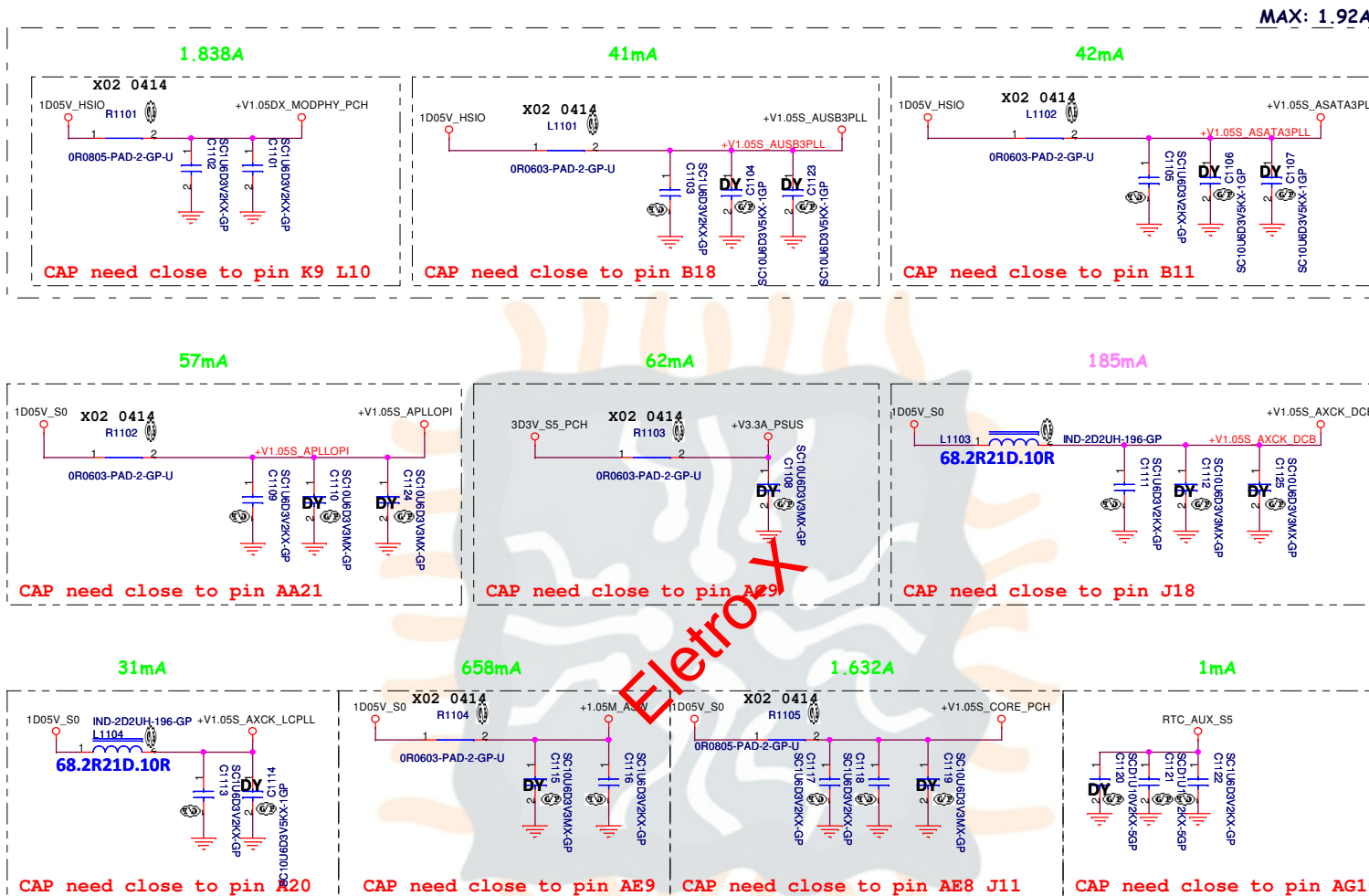
<Core Design>



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Title		CPU (Power CAP1)	
Size	Document Number	Rev	
A3	Cottonwood	400	
Date:	Tuesday, June 17, 2014	Sheet	10 of 103





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Title

CPU (Power CAP2)

Size
A3

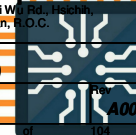
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Cottonwood

Date: Tuesday, June 17, 2014

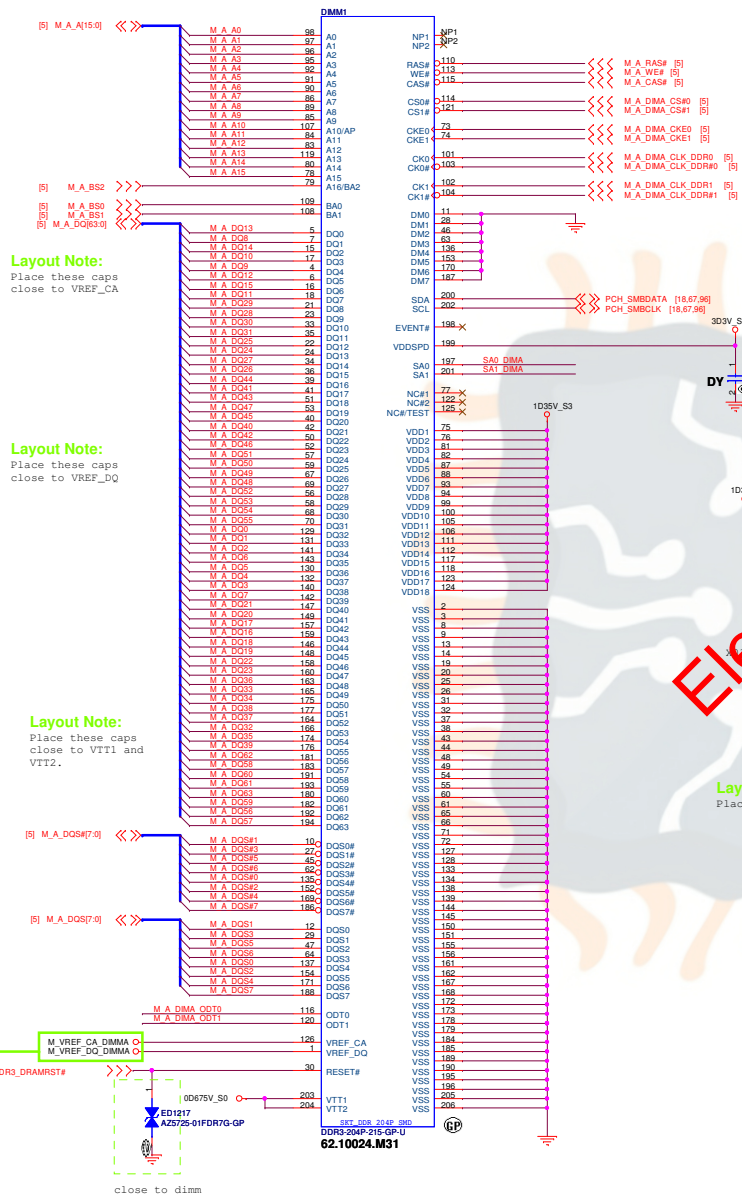
Sheet 11

of 103

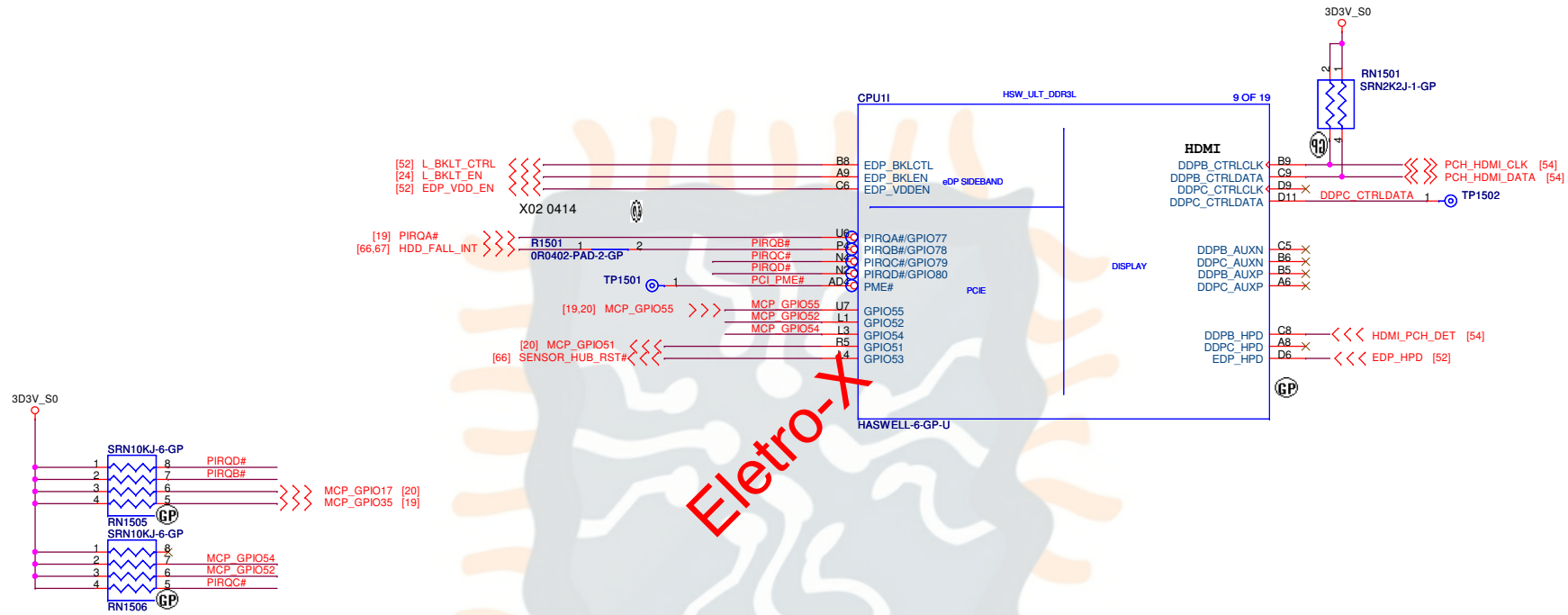


EEEtR0-2

SSID = MEMORY



SSID = CPU



ELECTRO-2

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Title: **PCH (EDP/GPIO/DDI)**

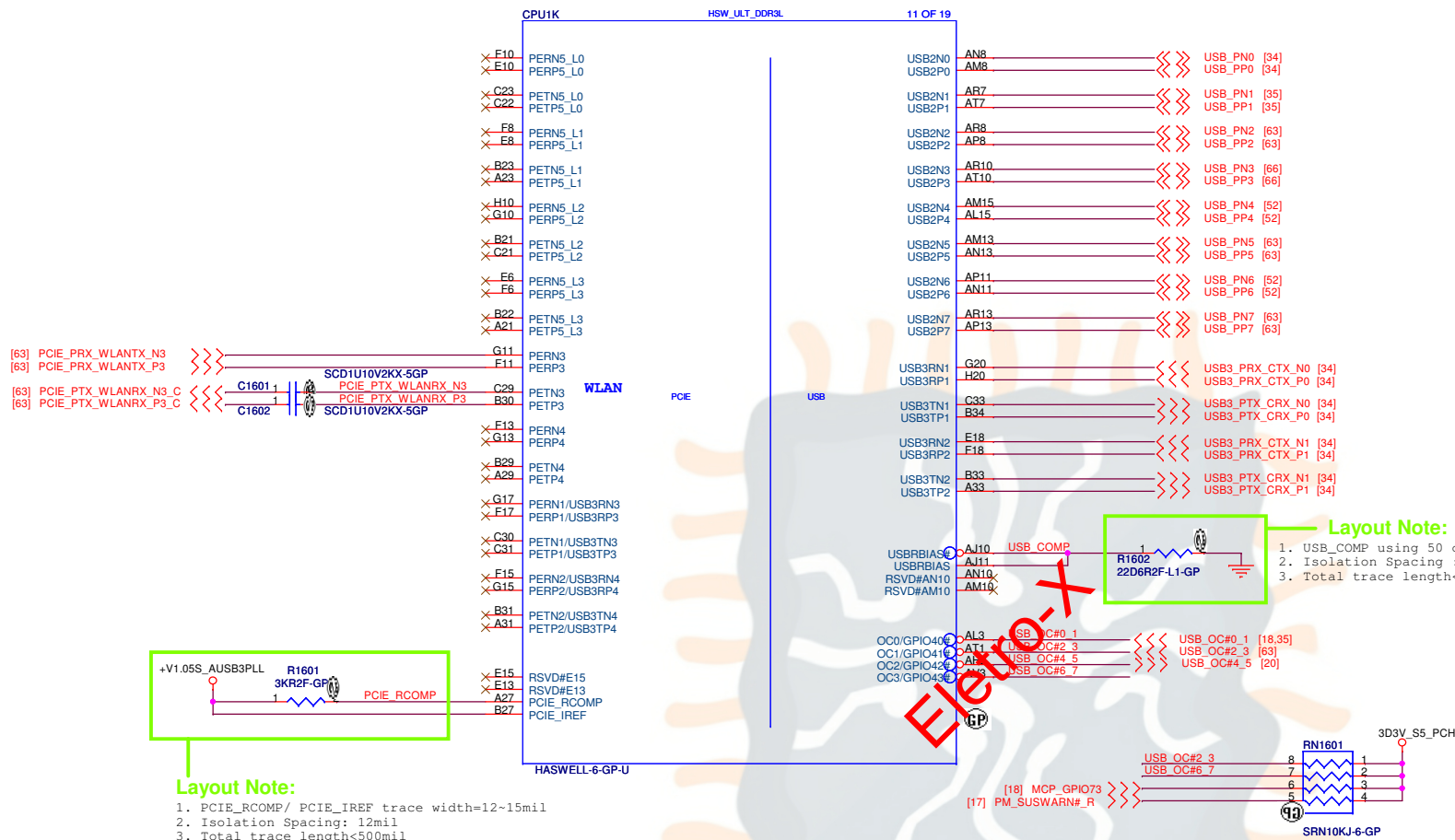
Size: A3 Document Number: **Cottonwood**

Date: Tuesday, June 17, 2014 Sheet: 15 of 103

SSID = PCH

USB 2.0 Table

Pair	Device
0	USB3.0 port2
1	USB3.0 Port1 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	N/A	
5 (L0~L3)	N/A	
6 (L3)	HDD	SATA0
6 (L2)	N/A	SATA1
6 (L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

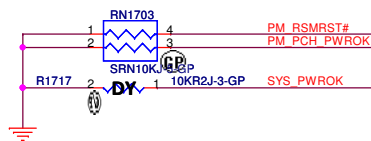
SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU	GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD		

<Core Design>



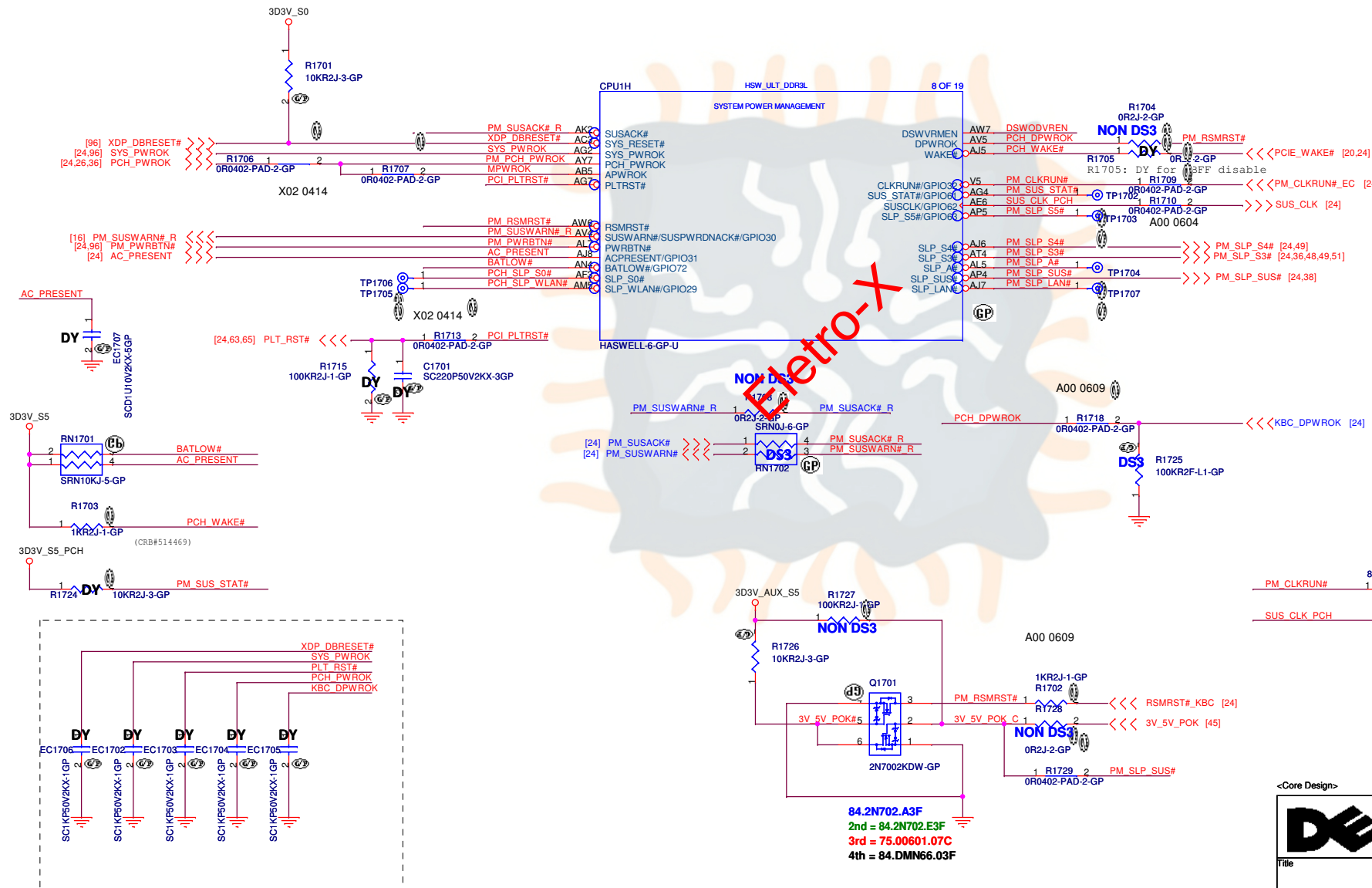
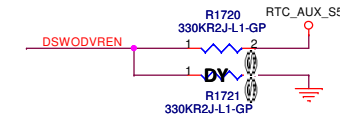
Title		PCH (PCIE/USB)	
Size A3	Document Number	Cottonwood	
Date: Tuesday, June 17, 2014		Sheet 16	of 103

SSID = PCH



PCH strap pin:

On Die DSW VR Enable	
DSWODVREN	Low = Disable ★ High = Enable (default)

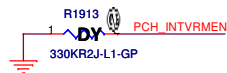


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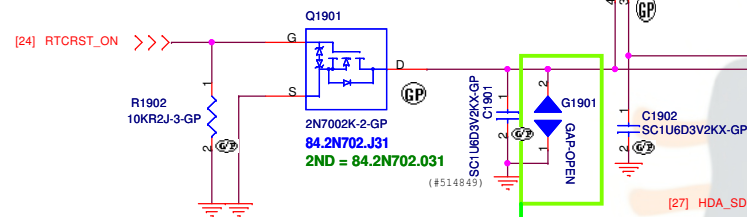
DELL		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Neihu, Taipei Hsien 221, Taiwan, R.O.C.			
PCH (PM)			
Cottonwood			
Title	Document Number	Sheet	17
Date: Tuesday, June 17, 2014			

Eletro-X

SSID = CPU



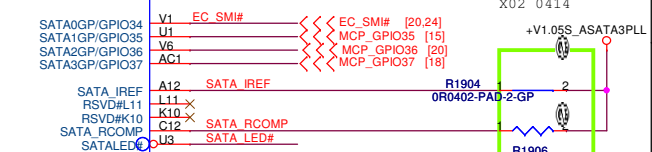
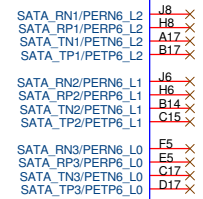
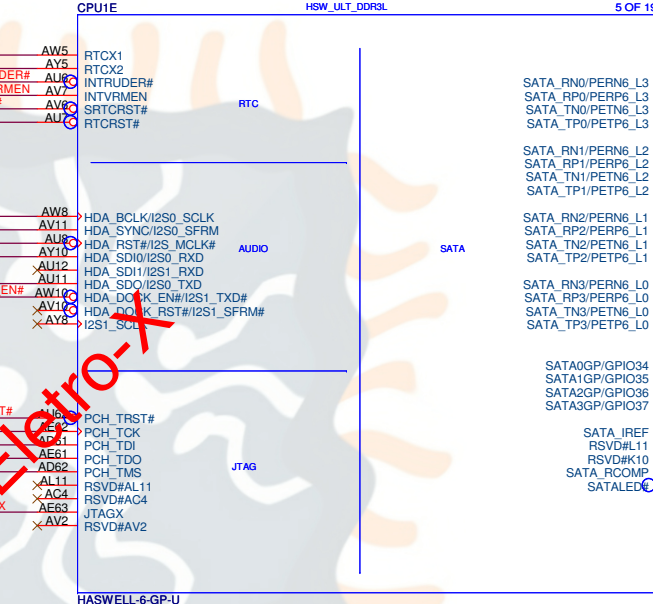
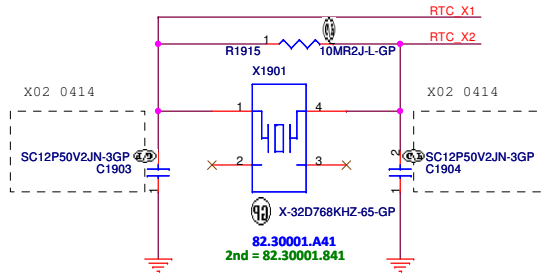
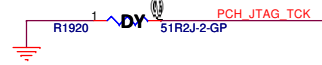
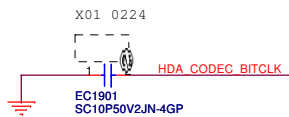
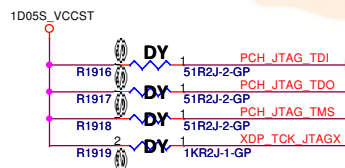
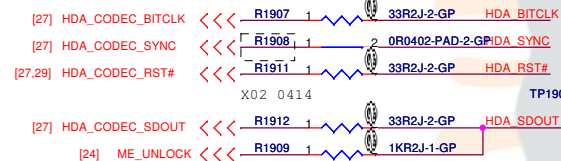
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*



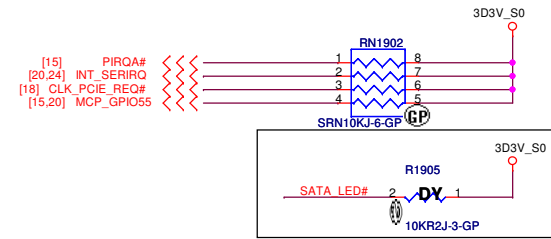
Layout: Place at the open door area.

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.



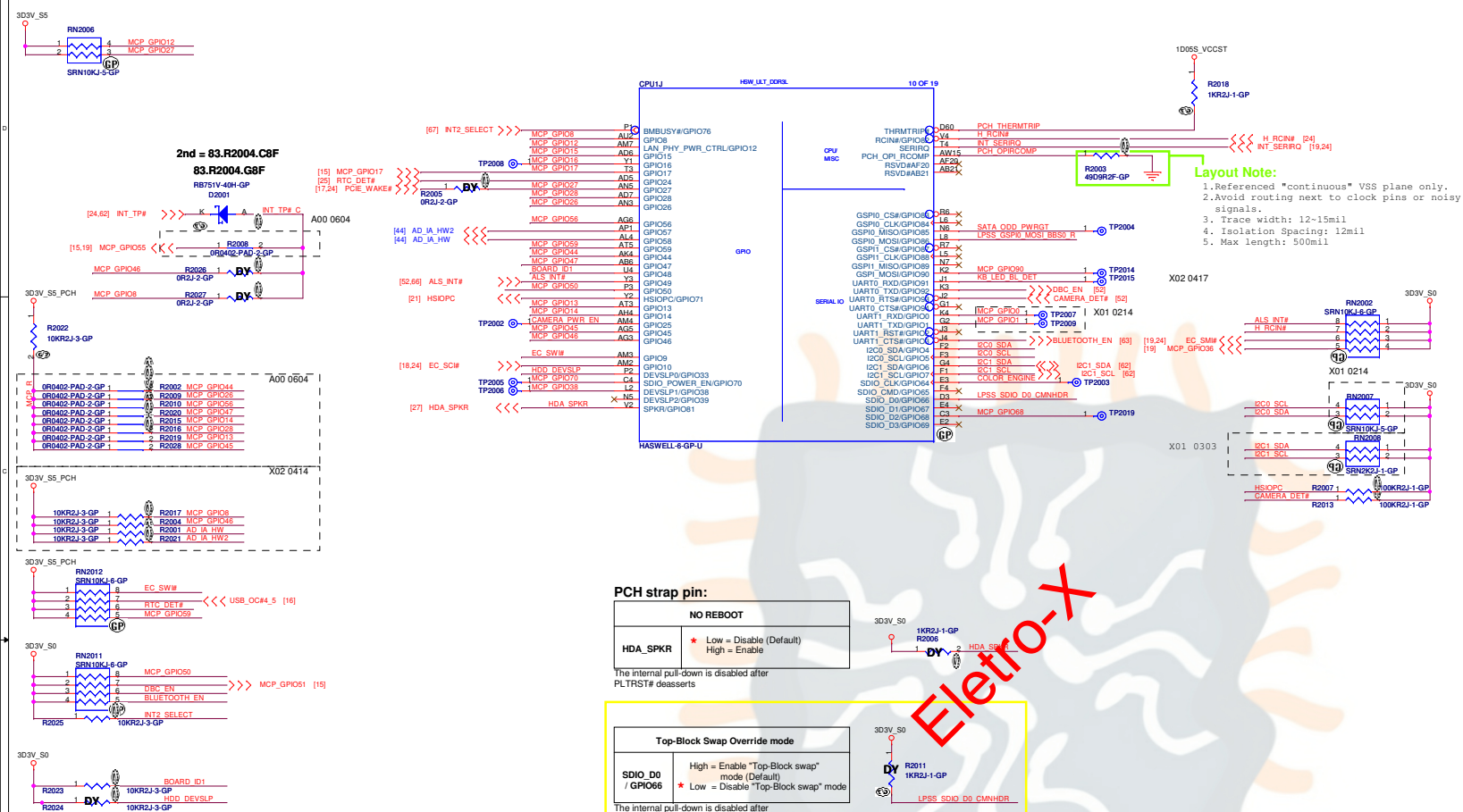
<Core Design>



Title		PCH (RTC/SATA/HDA/JTAG)		
Size	Document Number	Rev		
A3	Cottonwood	A00		
Date: Tuesday, June 17, 2014		Sheet	19	104

ECET-R0-0

SSID = CPU



PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	<p>High = Enable "Top-Block swap" mode (Default)</p> <p>★ Low = Disable "Top-Block swap" mode</p>

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality	
GPIO15	★ Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

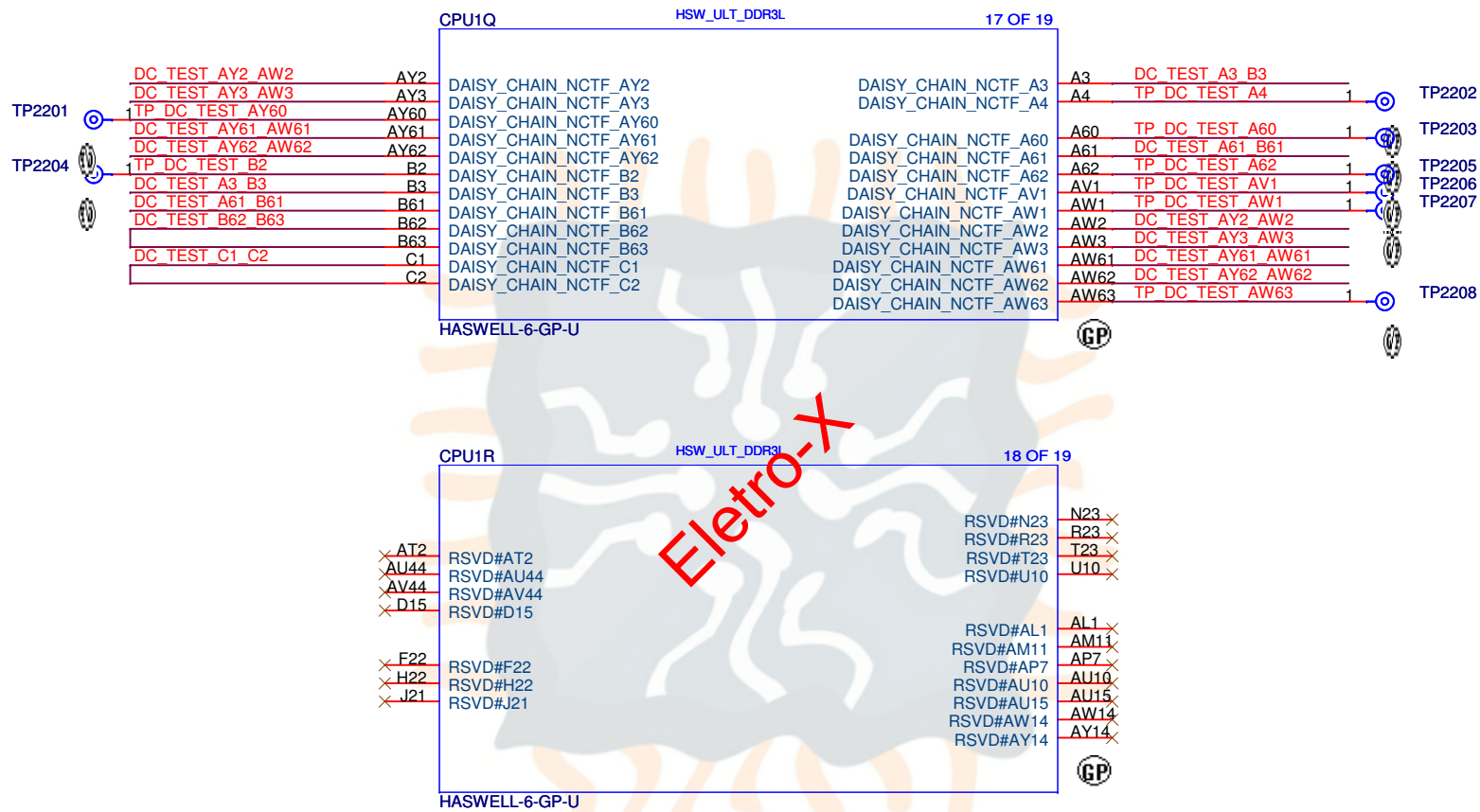
The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts


Need double confirm, GPIO table set to GPI if that's needed PH or PL

SSID = PCH



EEETRO-2

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Title

CPU (RSVD)

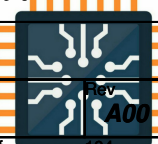
Size
A4

Document Number
Cottonwood

Date
Tuesday, June 17, 2014

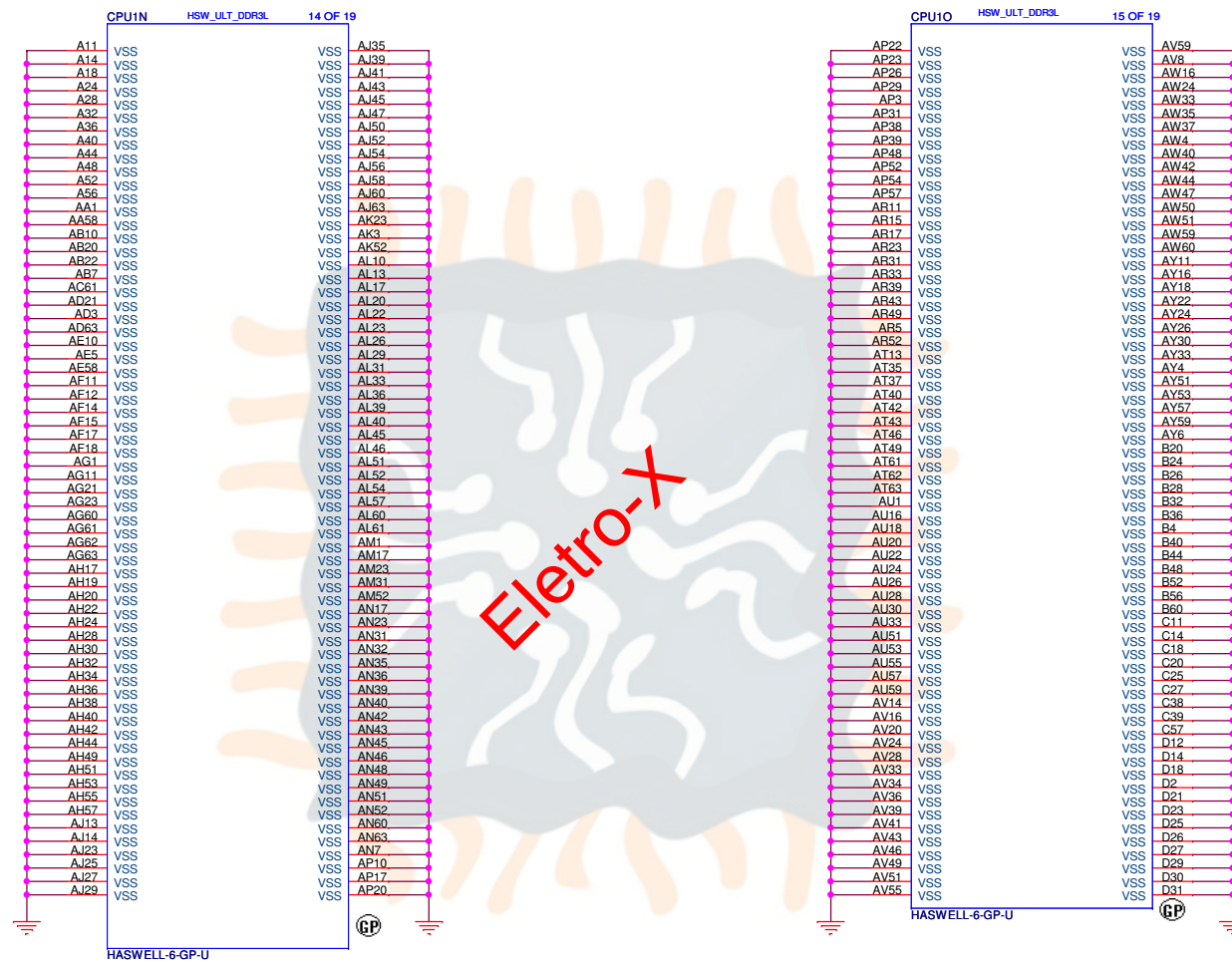
Sheet
22

of
104



Rev
A00

SSID = PCH



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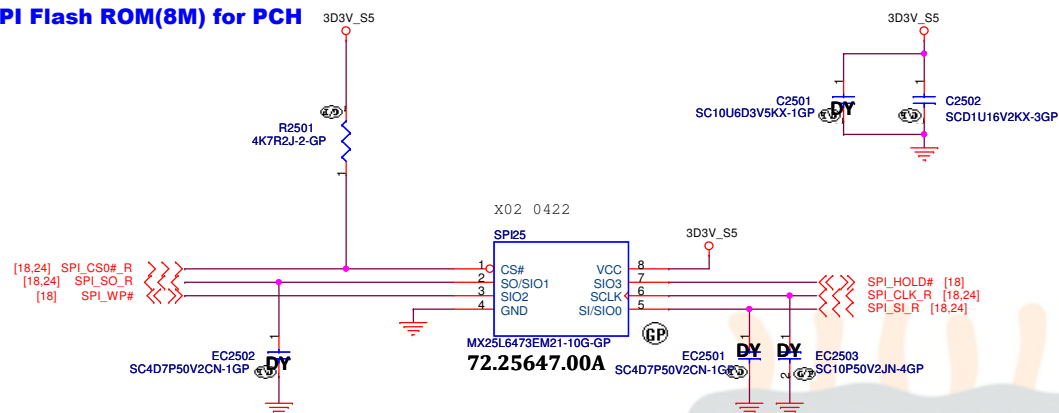


Title		CPU(VSS)	
Size	Document Number	Cottonwood	
A3			
Date:	Tuesday, June 17, 2014	Sheet	23

ELECTRO-2

SSID = Flash.ROM

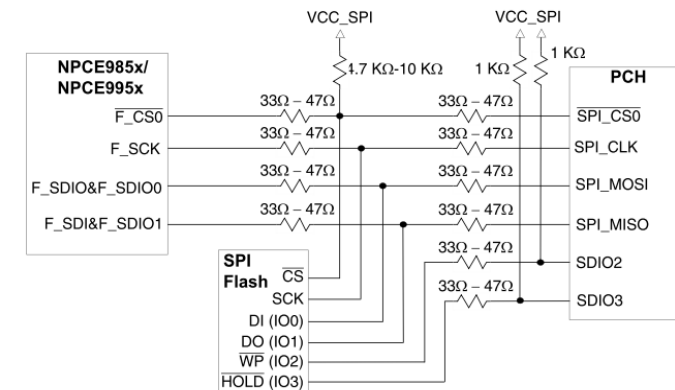
SPI Flash ROM(8M) for PCH



X01 0219

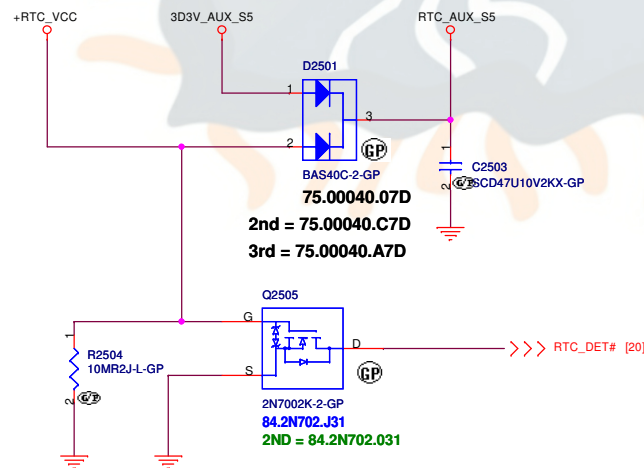
Source	QUAD/DUAL fast read	DUAL fast read
72.25647.00A	o	o
072.25864.0001	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

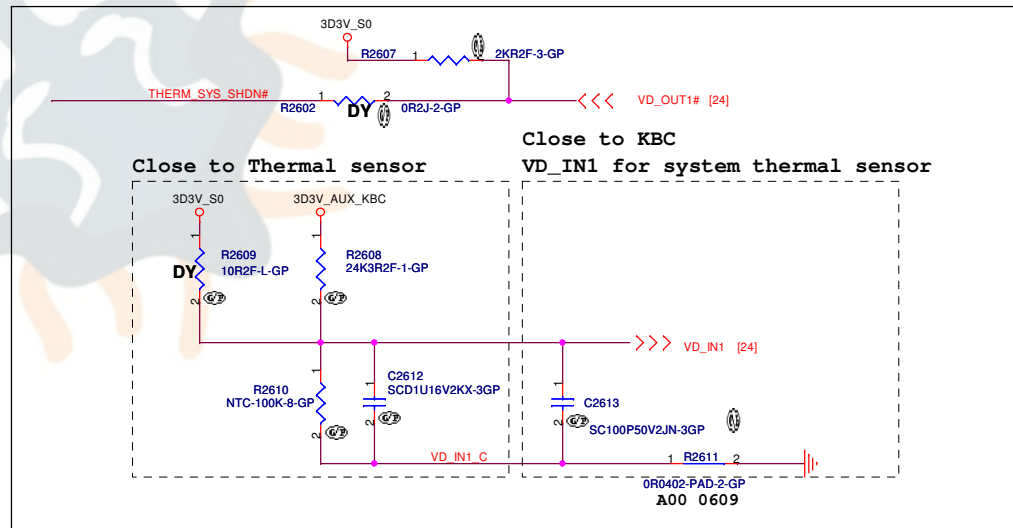
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wai Rd., Taipei,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash/RTC**
Size A3 Document Number: **Cottonwood**
Date: Tuesday, June 17, 2014 Sheet 25 of 103

SSID = Thermal



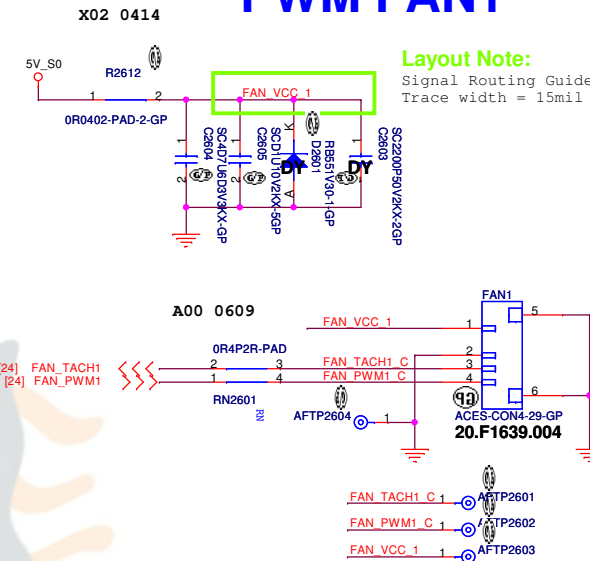
TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



PWM FAN1

Layout Note:

Signal Routing Guideline:
Trace width = 15mil



KBC T8

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title **THERMAL NCT7718W/Fan**

Size A3	Document Number Cottonwood
------------	--------------------------------------

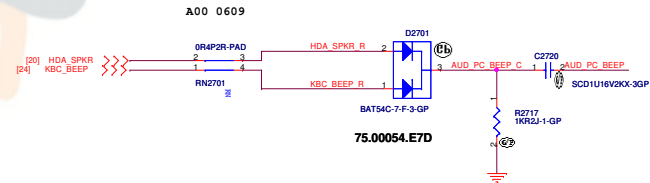
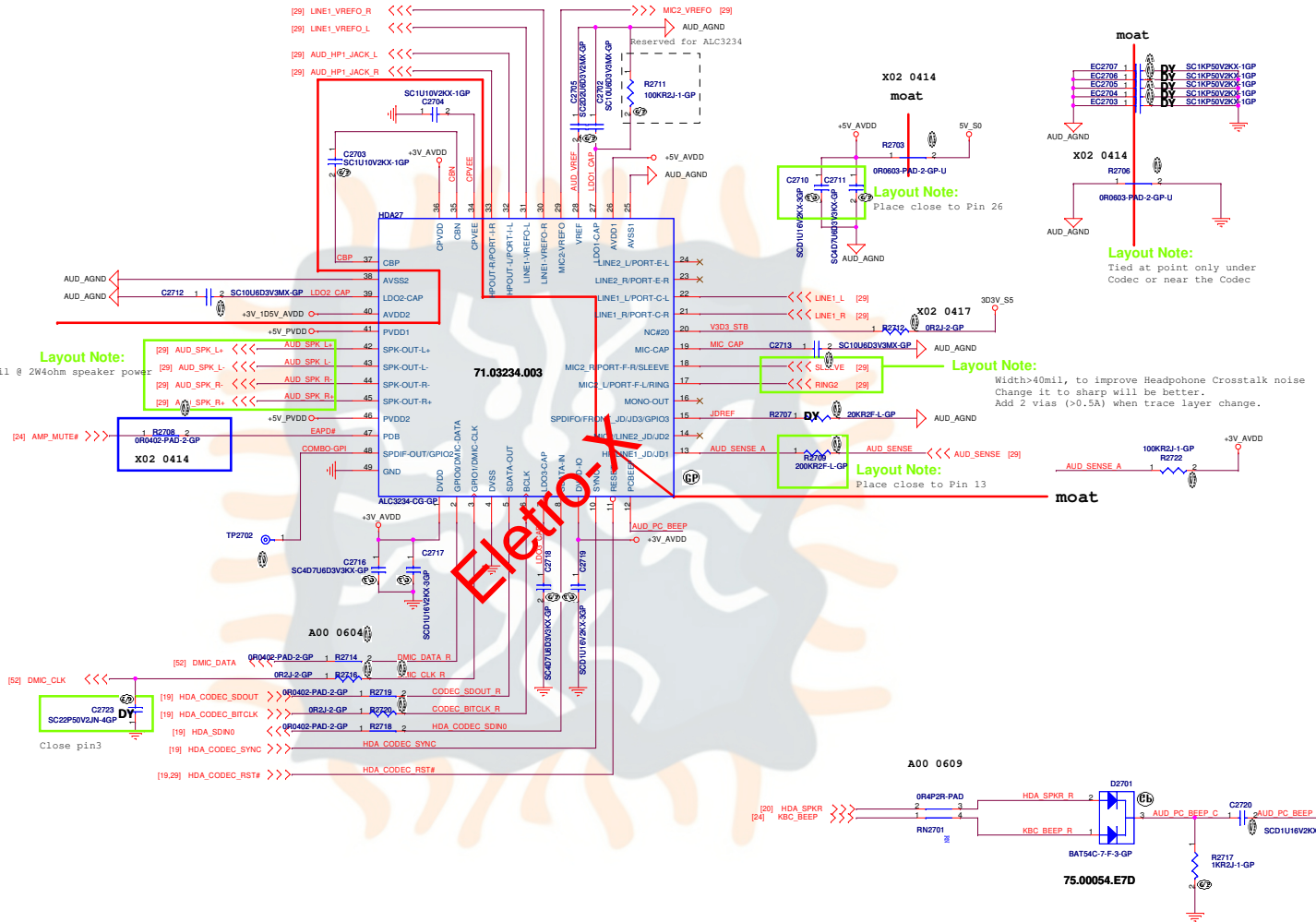
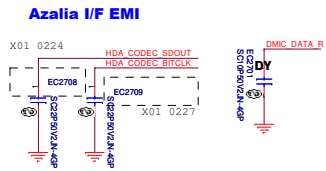
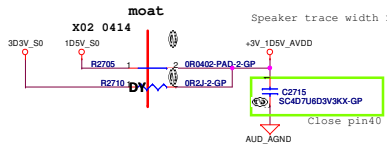
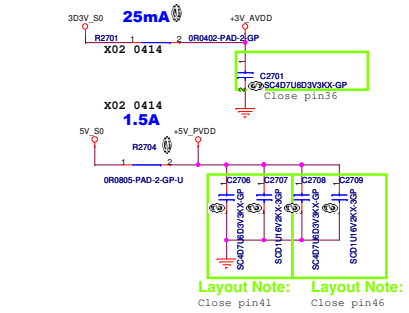
Date: Tuesday, June 17, 2014

Sheet 26

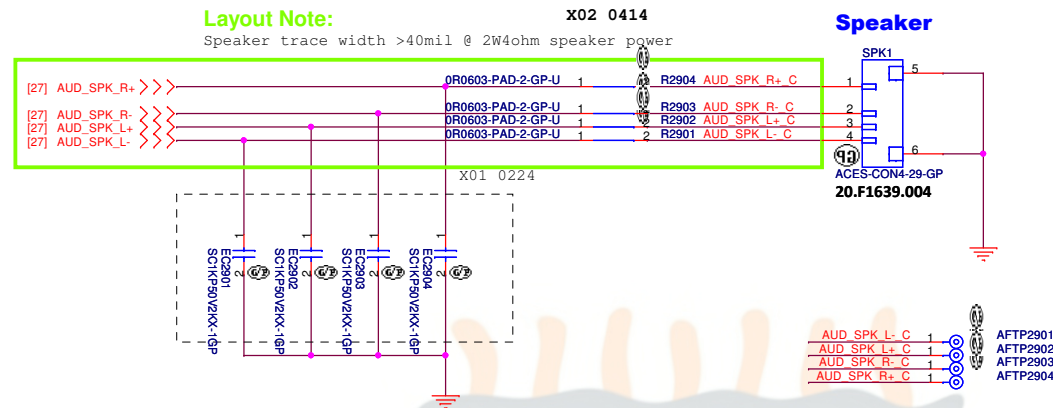
Rev
A00

104

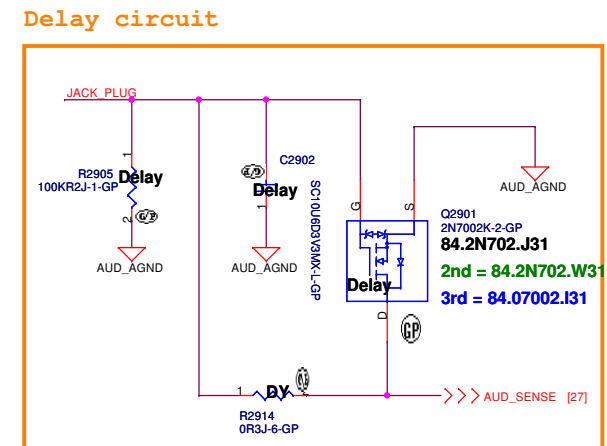
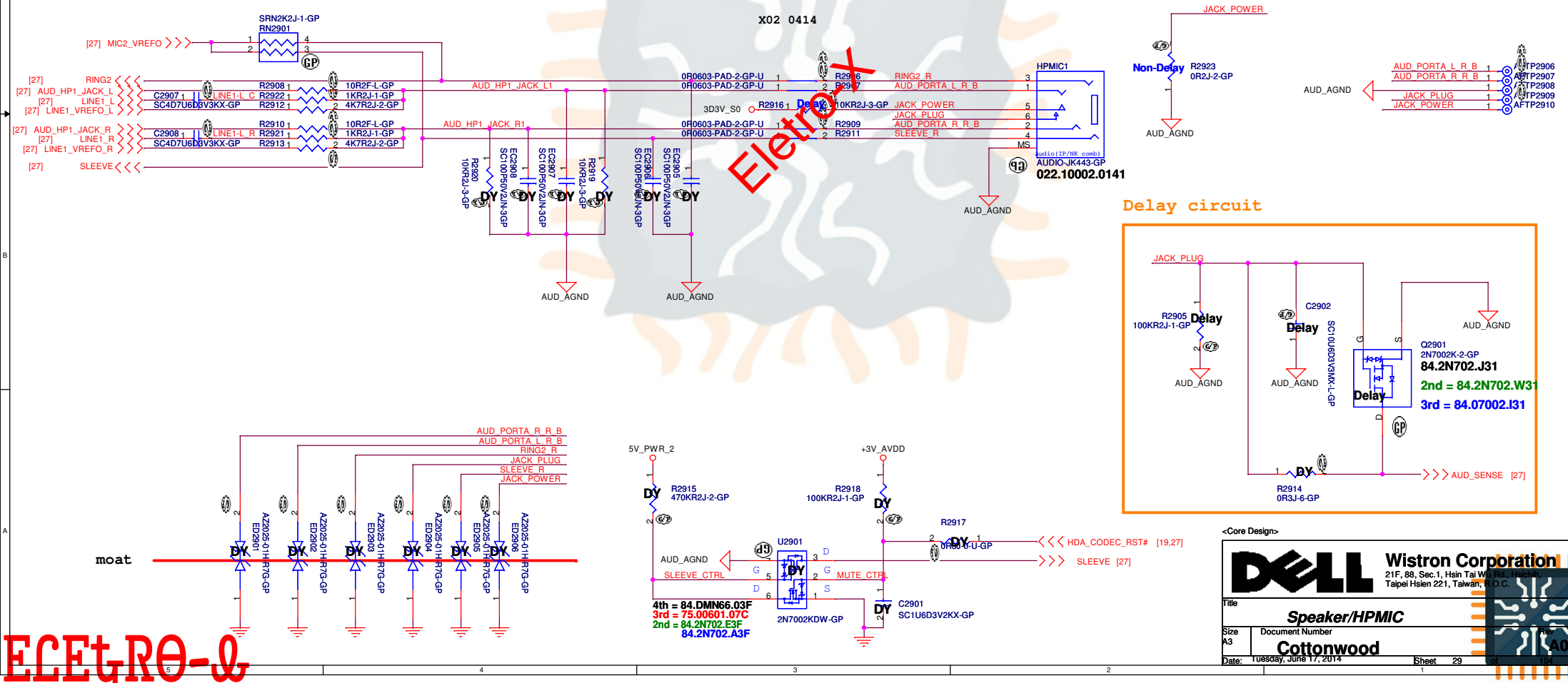
SSID = AUDIO



SSID = AUDIO

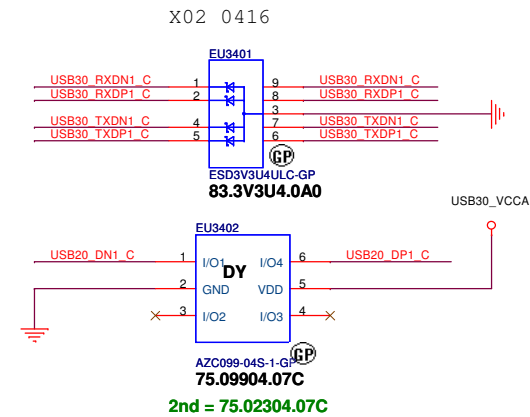
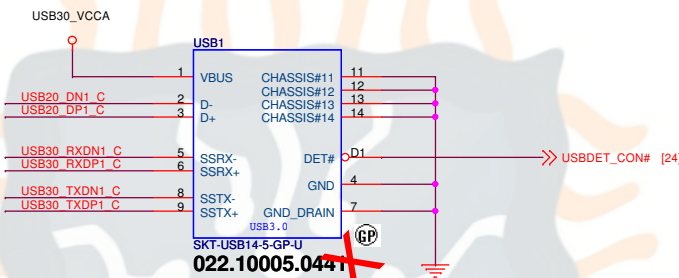
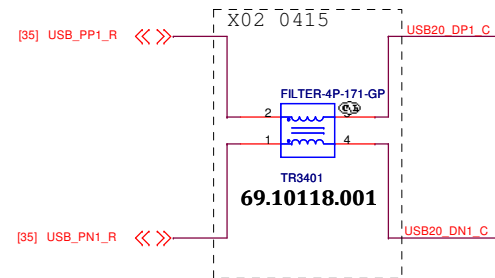
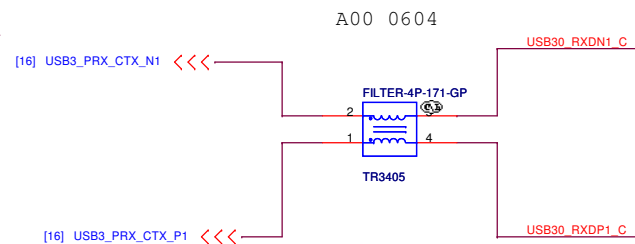
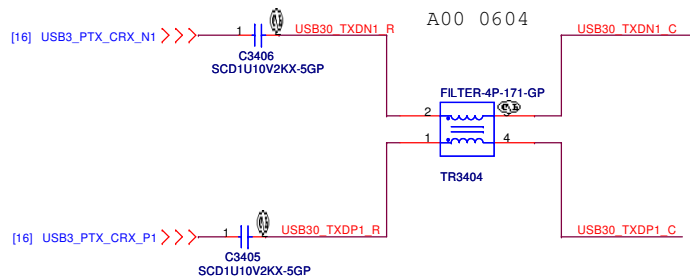


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



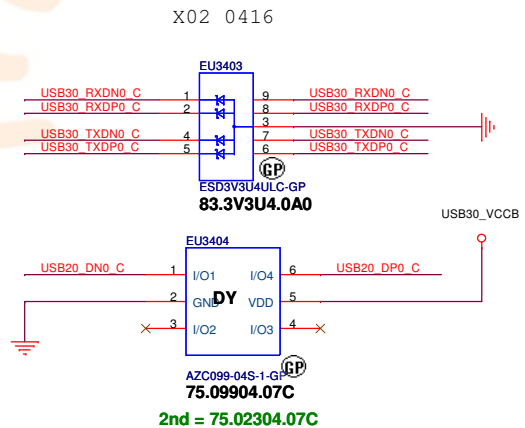
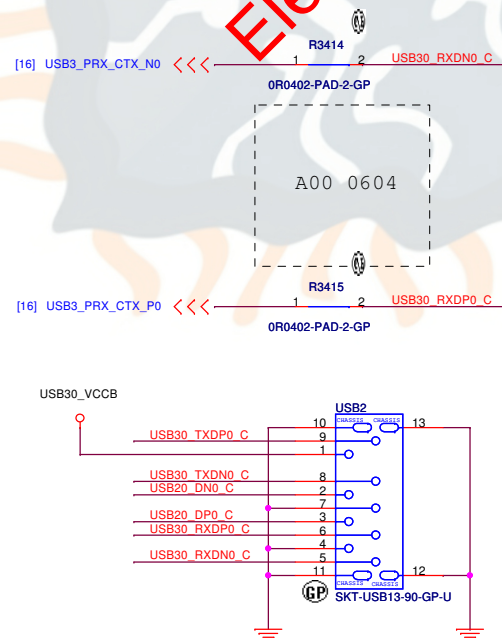
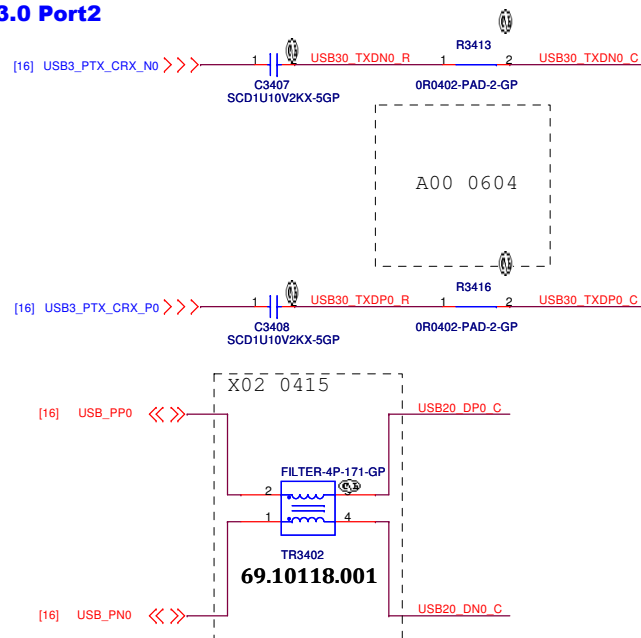
SSID = USB

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



<Core Design>

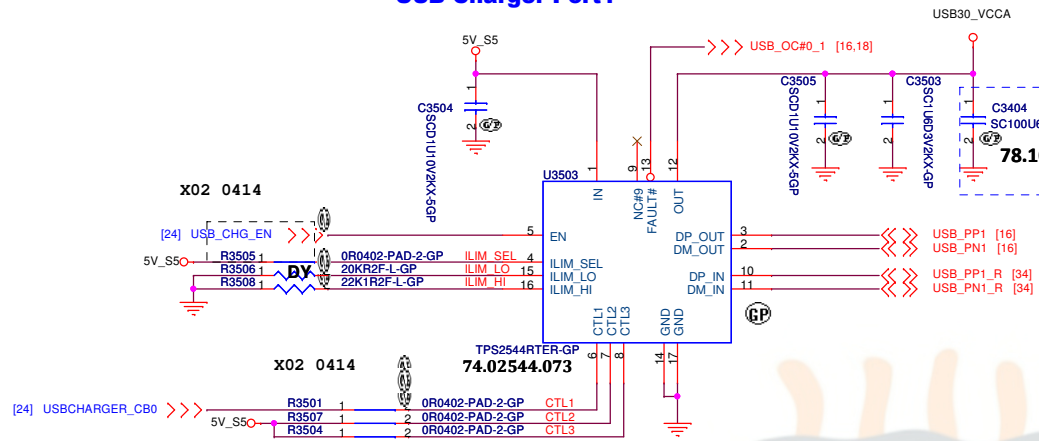
DELL Wistron Corporation
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Title: **USB 3.0**

Size: A3 Document Number: **Cottonwood**

Date: Tuesday, June 17, 2014 Sheet: 34 of 103

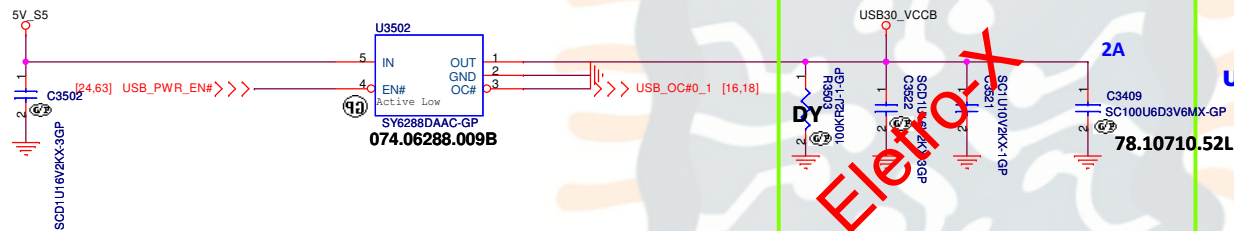
USB Charger Port1



If MLCC is used as Main Source.
Inform Layout team to remark Pin 1 as positive.
In case MLCC shortage and other type of Cap With Polarity Is Used.

Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

Layout Note: Close CON1

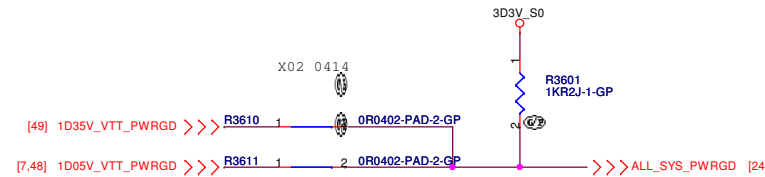
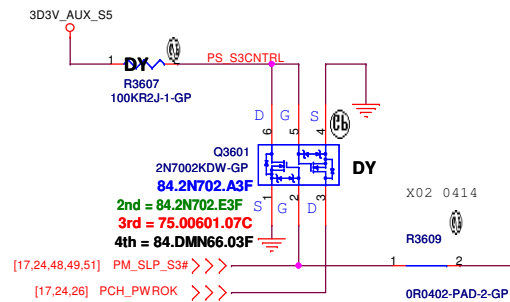


USB3.0 Port2


```
SSID = Reset.Suspend
```

Power Good

ROSA Run Power

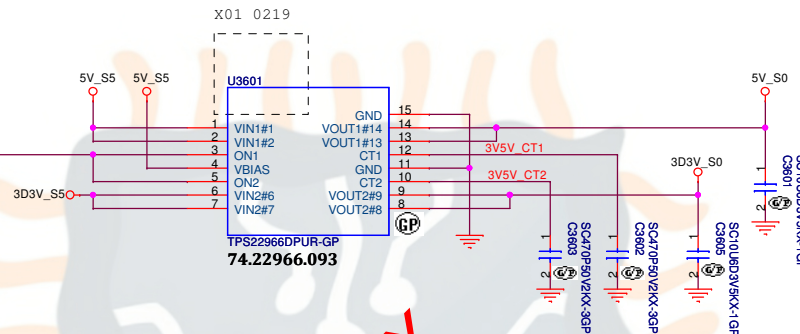


5V_S0

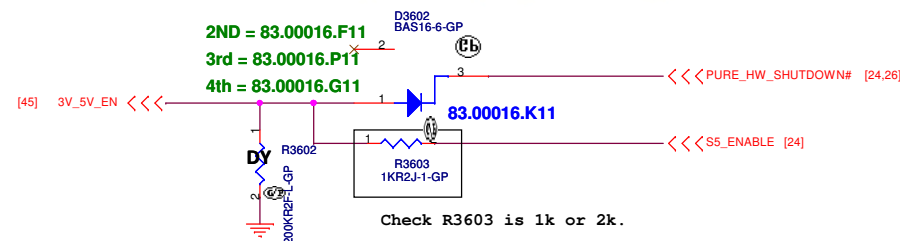
5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A



Eleto-X



<Core Design>



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Title

Size

Document Number

Cottonwood

Date: Tuesday, June 17, 2014

Sheet 36

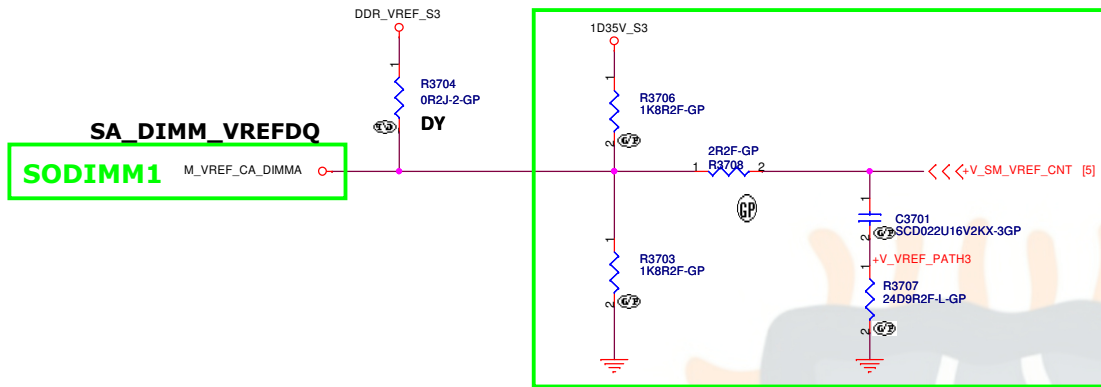
f

4

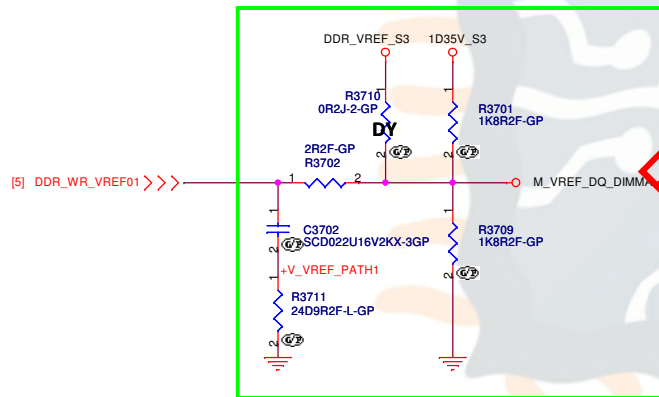
ECETRO-2

SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMM1



Layout Note:
Place Close SO-DIMM1



Eletron-X

ELETRON-X

<Core Design>



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Title

S3 Reduction Circuit

Size
A3

Document Number

Cottonwood

Date: Tuesday, June 17, 2014

Sheet 37

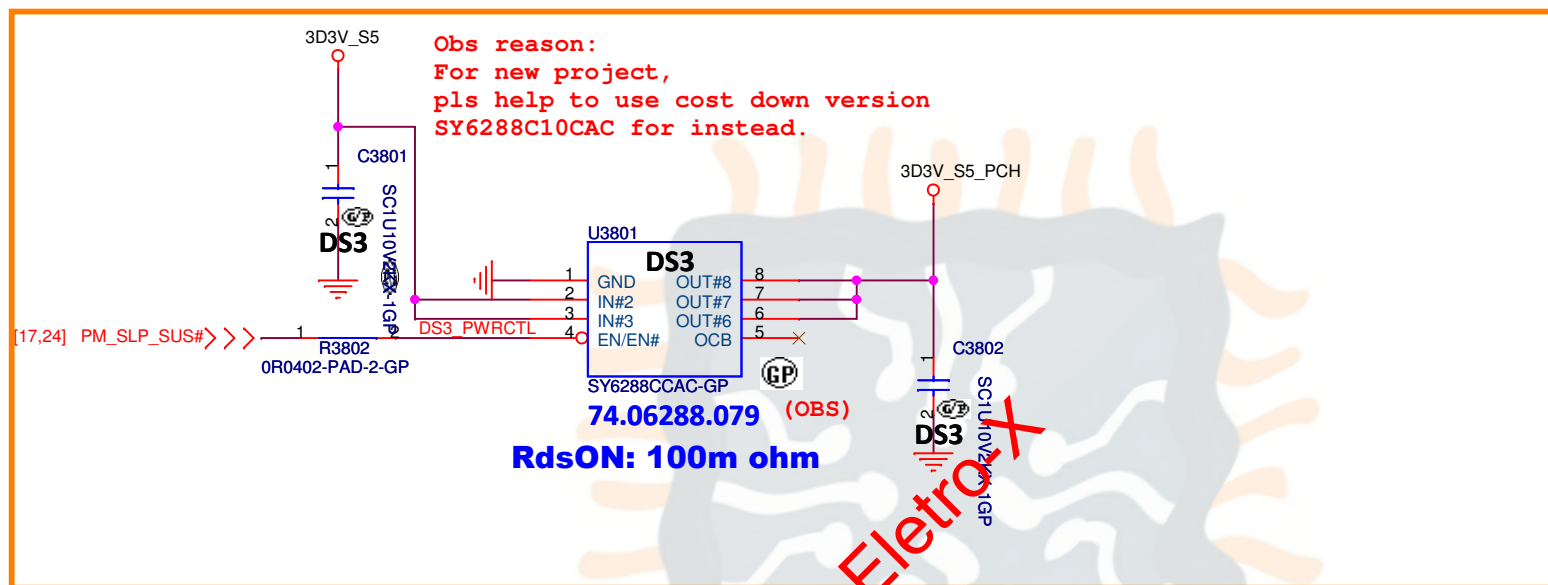
Rev

A00

103



Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.



DS3

<Core Design>

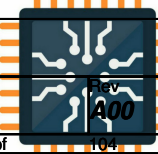


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Title **DSW**

Size A4 Document Number **Cottonwood**

Date: Tuesday, June 17, 2014 Sheet 38 of 104



ELETRO-2

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

$I_d = -9.6A$
 $Q_g = -25nC$
 $R_{ds(on)} = 18 \sim 30m\Omega$

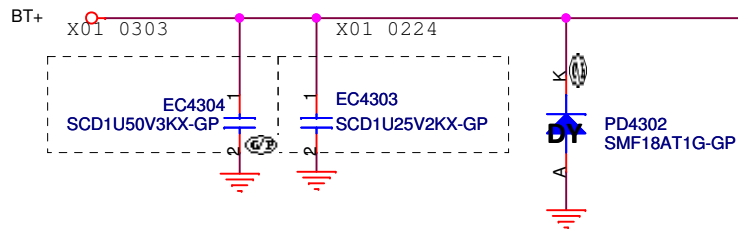
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

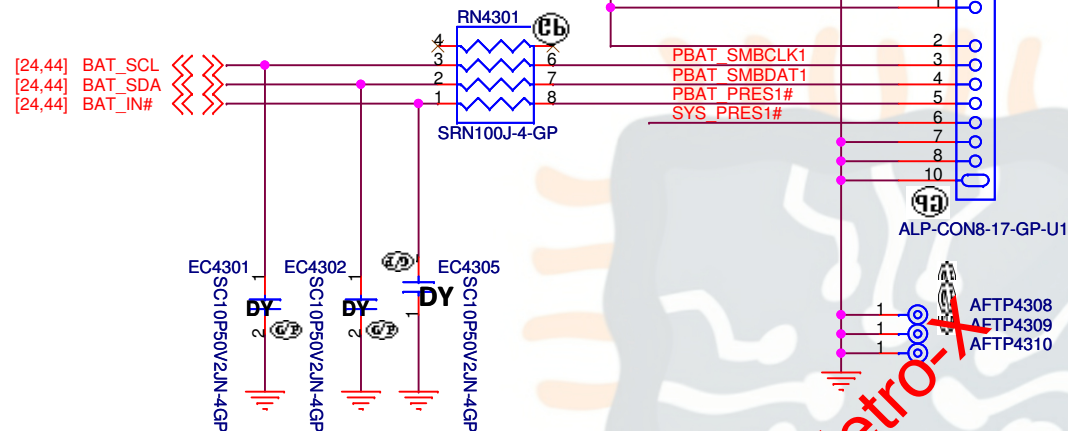
Title		DCIN	
Size	Document Number	A00	
A3		Cottonwood	
Date:	Tuesday, June 17, 2014	Sheet	42 of 103

ELETR0-2

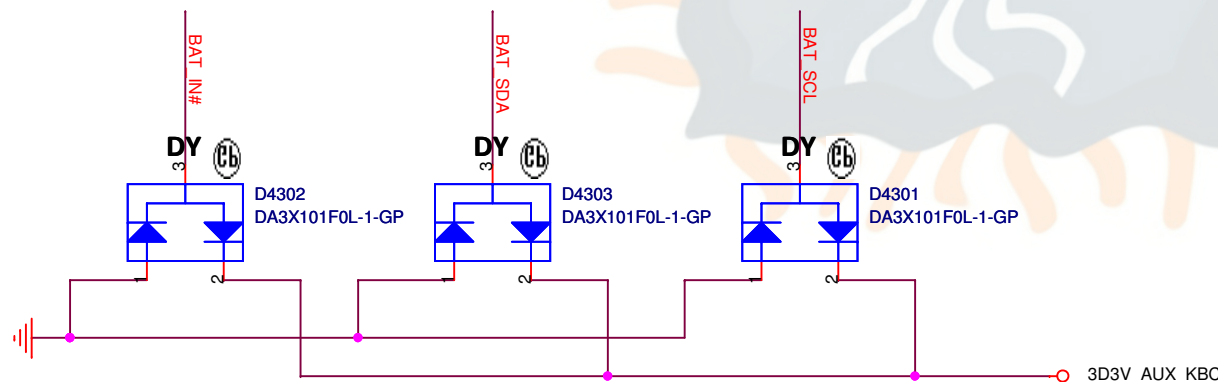
SSID = PWR.Support



Batt Connector



Placement: Close to Batt Connector



75.03101.07D

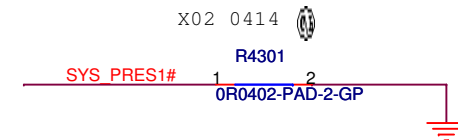
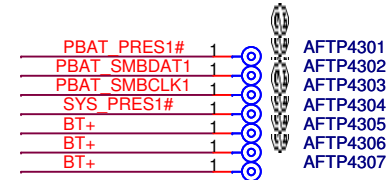
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3rd = 83.00099.M11

75.03101.07D

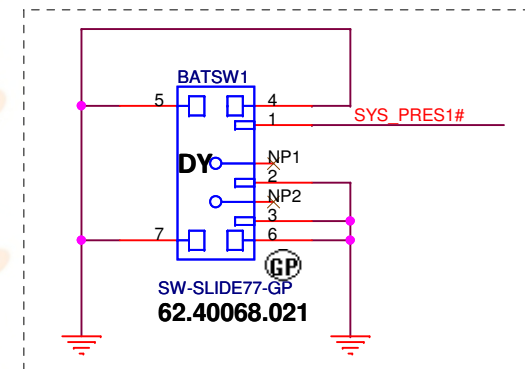
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D

2nd = 83.00099.K11
3rd = 83.00099.M11



X01 0226



<Core Design>



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Title

BATT CONN

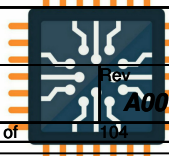
Size
A4

Document Number

Cottonwood

Date: Tuesday, June 17, 2014

Sheet 43 of 104



ECE+R0-2

KBC FOR DT MODE
CHECK EE PULL HIGH

CHECK EE
follow customer circuits.

Customer Request

Close PR4443

BATTERY MON

[M] BOOST_MON <<< [PR4443] [PR4443]

BOW CA

V _{REGH_REG}	REGN Regulator Voltage	V _{VCC} > 6.5V, V _{VACDET} = 0.6V	5.4	V
-----------------------	------------------------	---	-----	---

PU4406:
main source: 84.03660.037

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

CHECK PM ADAPTER TYPE
And setting adapter type

(AD_TA_HW)

(AD_TA_HW_2)

ADAPTER TYPE	AD_TA_HW	AD_TA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

©Core Design

SSID = PWR.Plane.Regulator_5v3p3v

Design Current=4A
6A<OCP>6.5A

Design Current=6.7A
10.6A<OCP>12.5A

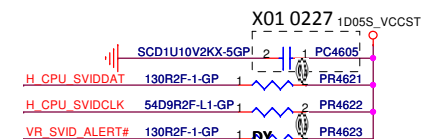
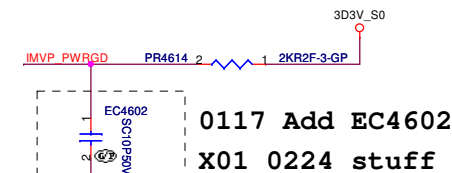
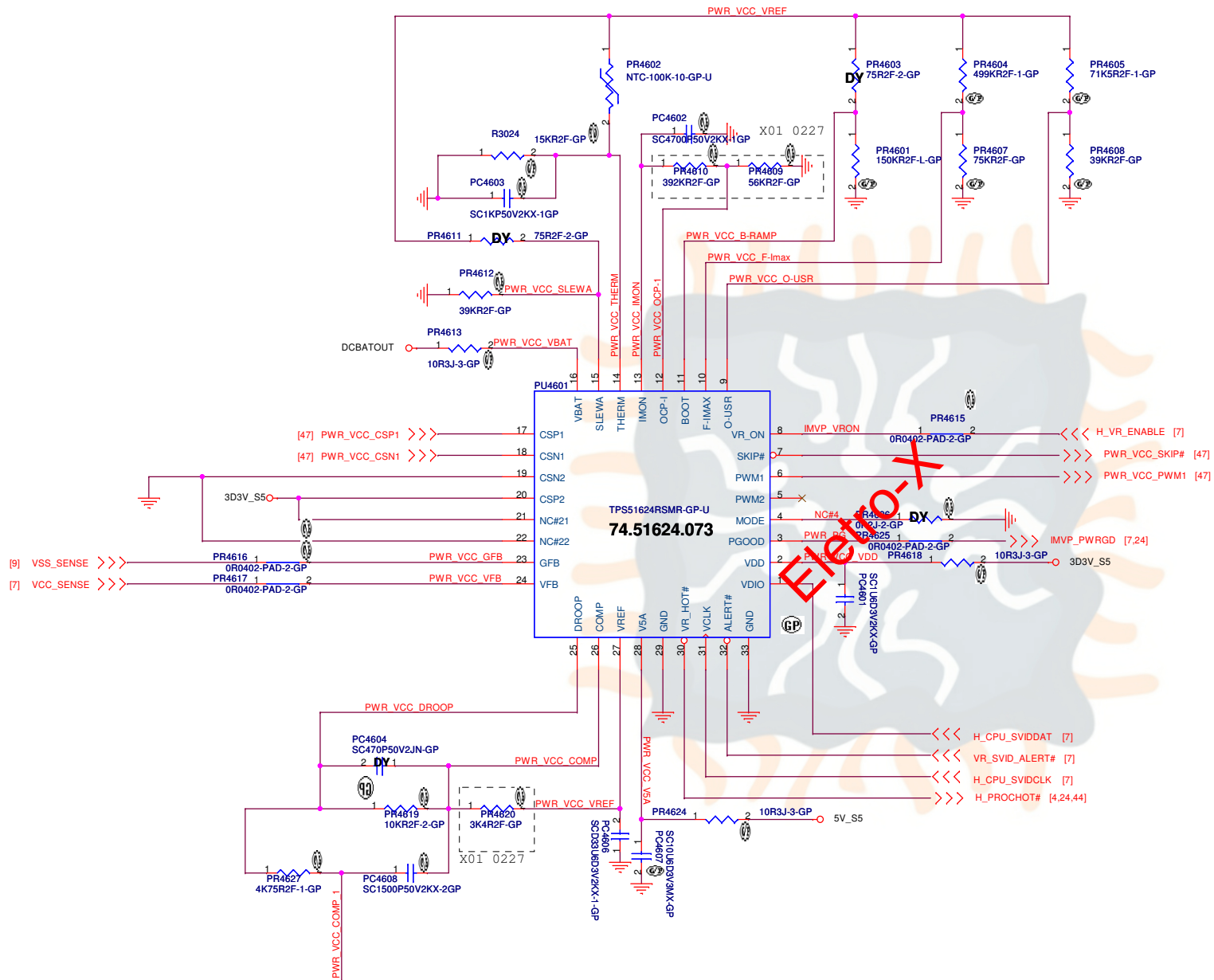
TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	64.9K	13K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKR 4.7UH PCMO63T-4R7MS Cyntec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL/NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKR 2.20 PCMO63T-2R20N 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL/NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

SSID = CPU.Regulator



		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCF	PR4609	150K	75K
IMON	PR4610	680K	422K
Load time	PR4620	2.8K	3K

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **046P TPS51624 CPUCORE(1/2)**

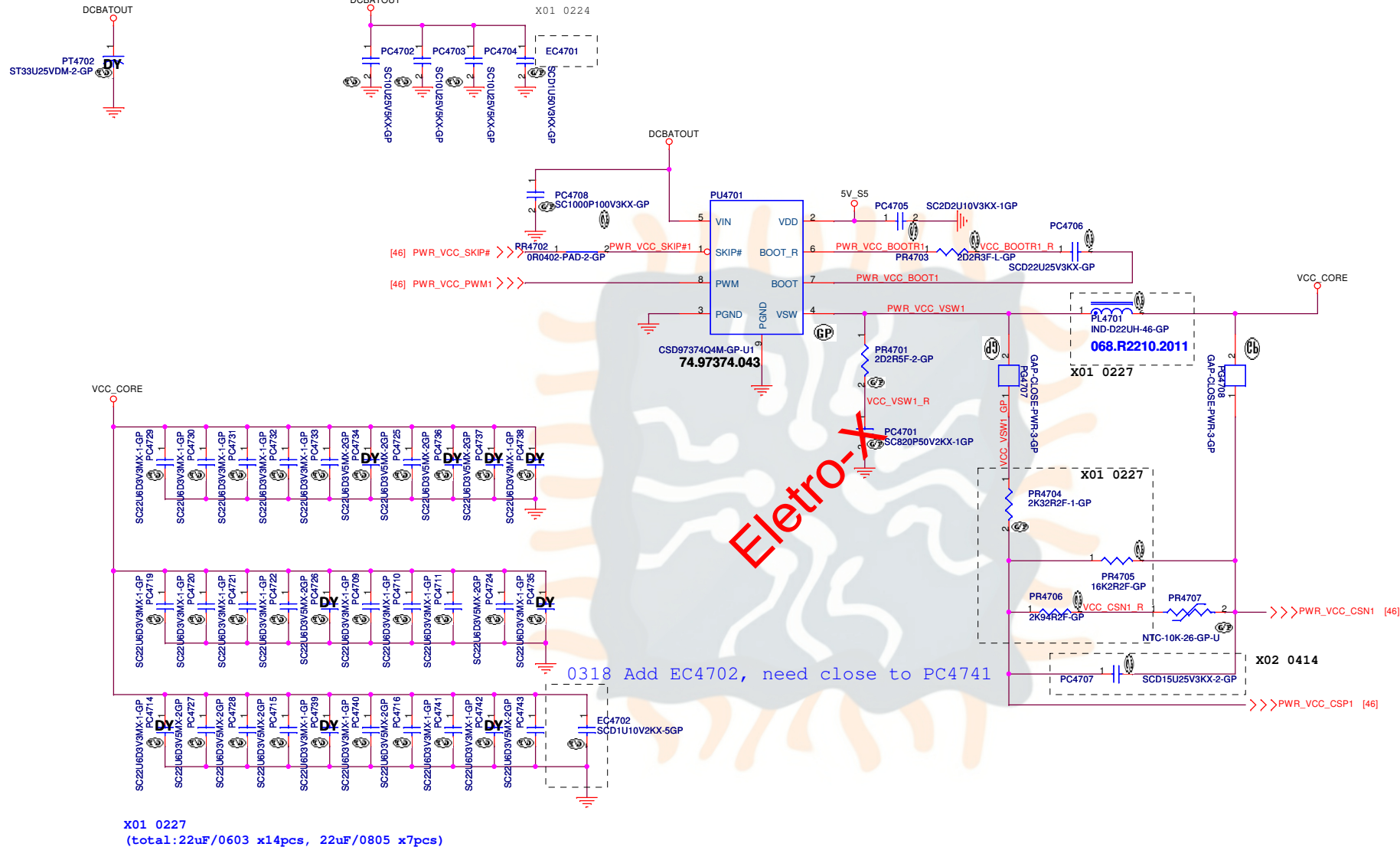
Size A3 Document Number: **Cottonwood**

Date: Tuesday, June 17, 2014 Sheet 46 of 100

EEEtR0-2

SSID = CPU.Regulator

For acoustic noise



<Core Design>

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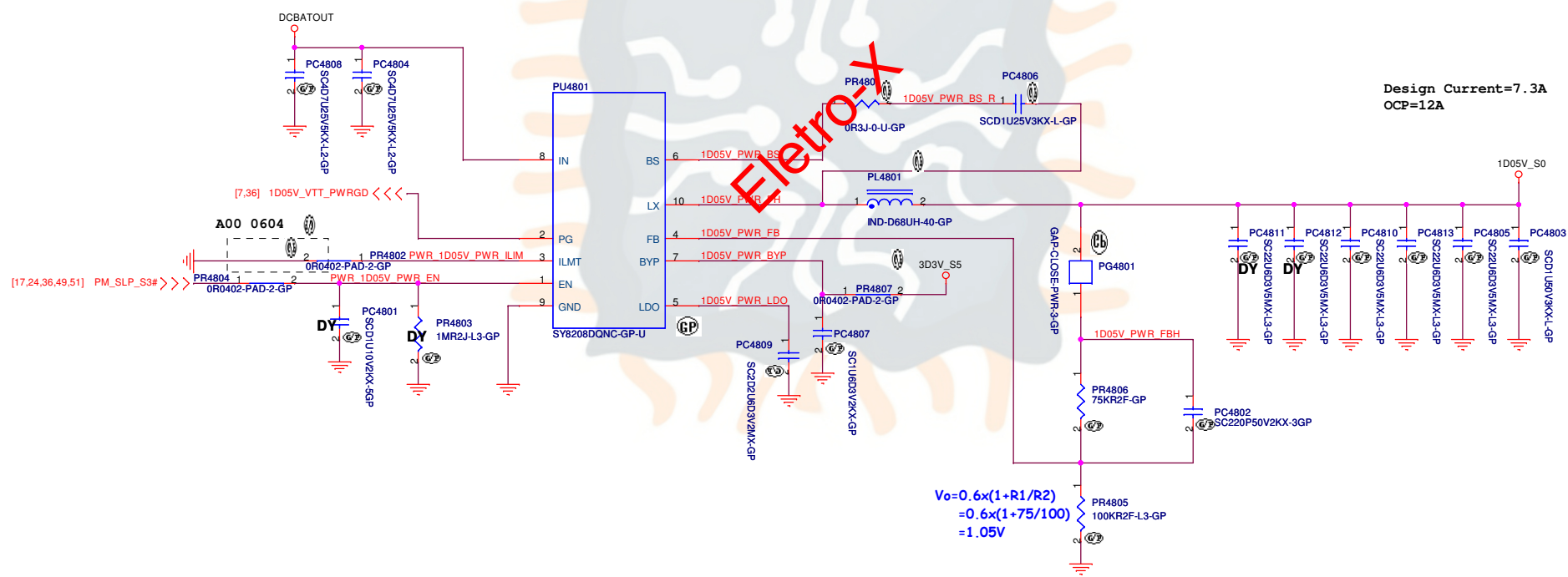
Title: **047P TPS51624 CPUCORE(2/2)**

Size: A3 Document Number: **Cottonwood**

Date: Tuesday, June 17, 2014 Sheet: 47 of 100

SSID = PWR.Plane.Regulator_1p05v

SY8208D for 1D05V



<Core Design>

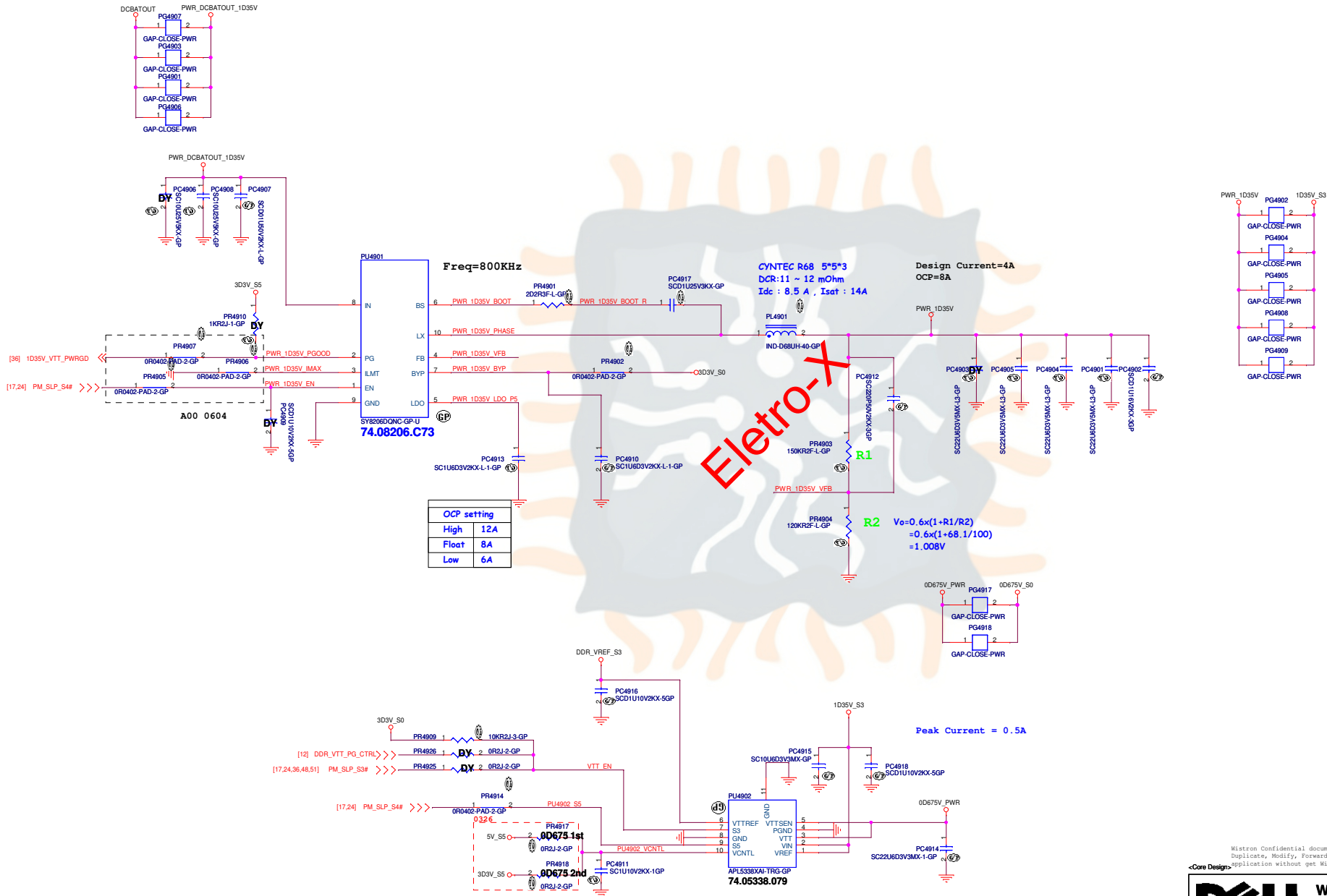
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	SY8208DQNC 1D05V		
Size	A3	Document Number	Cottonwood
Date	Tuesday, June 17, 2014	Sheet	48

Ref: A00

ELECTRO-2

SY8206D for 1D35V



If use 74.02997.B79, Stuff PR4918 and Dummy PR4917.

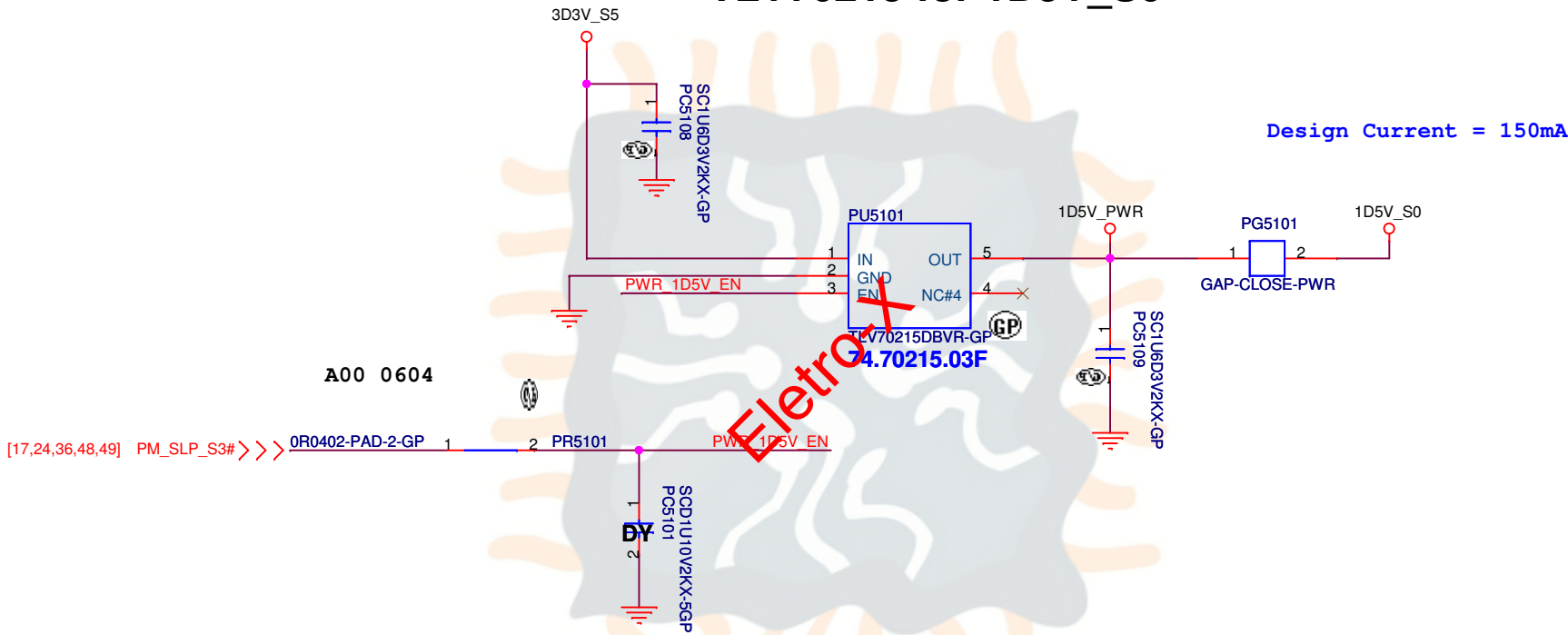
2nd source:
74.02997.B79

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SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0

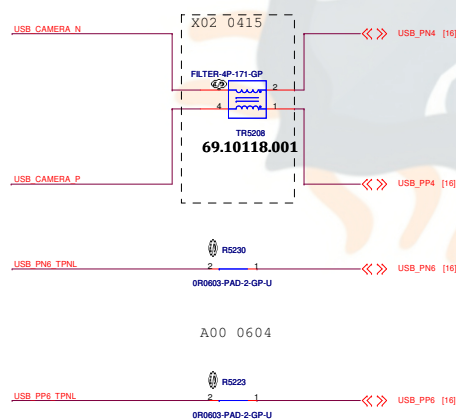
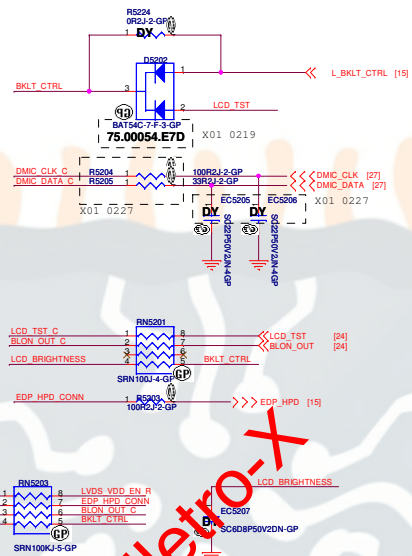
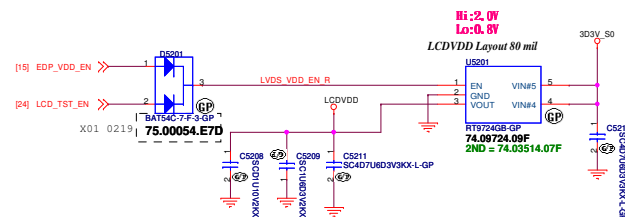
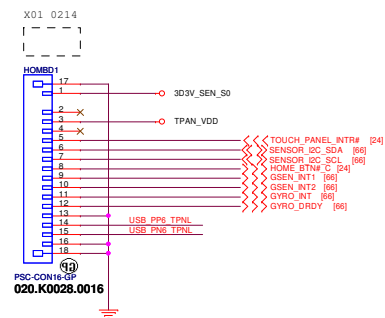


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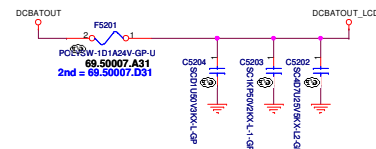
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		TPS51367 1D5V	
Size	Document Number	Cottonwood	
A4		Rev A00	
Date:	Tuesday, June 17, 2014	Sheet	51 of 104

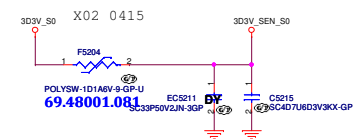
ECE+R0-2



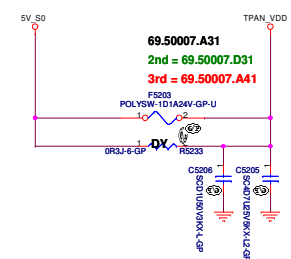
INVERTER POWER



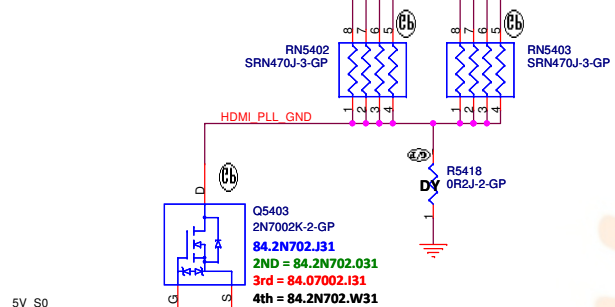
SENSOR POWER



TOUCH PANEL POWER



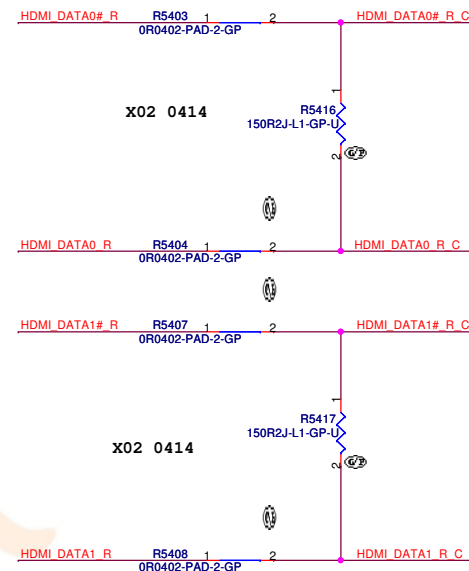
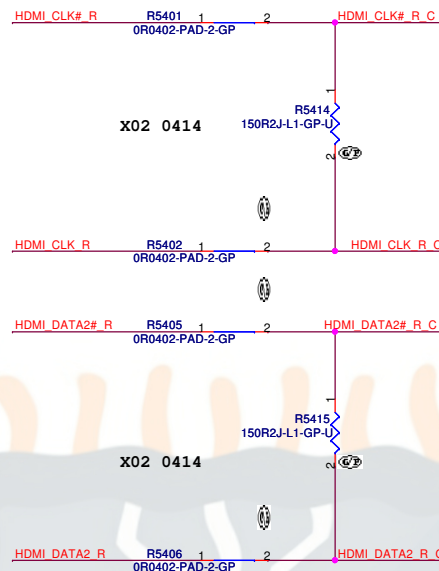
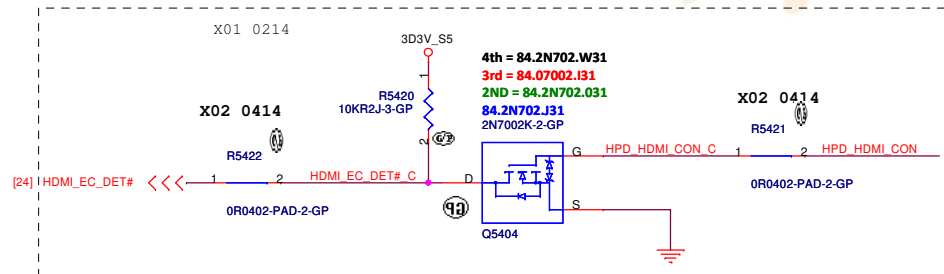
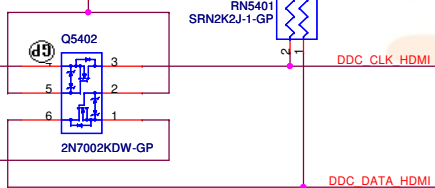
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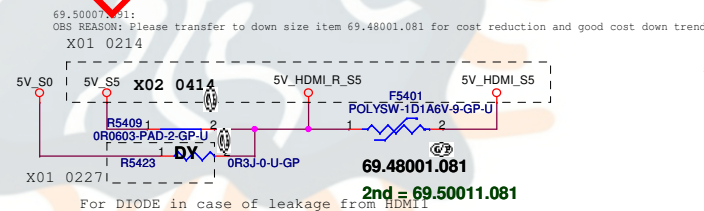
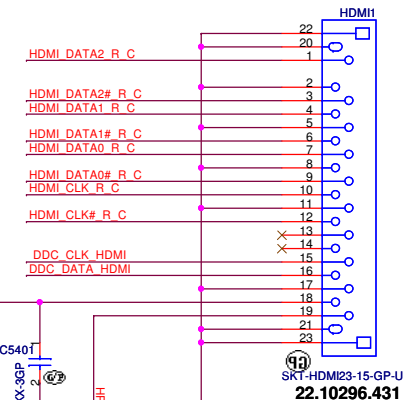
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

[15] PCH_HDMI_CLK >>>

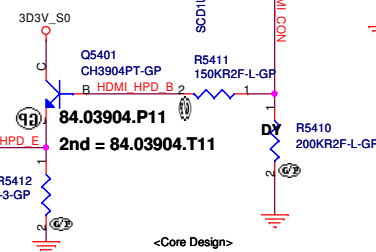
[15] PCH_HDMI_DATA <<<



HDMI CONN



[15] HDMI_PCH_DET <<<



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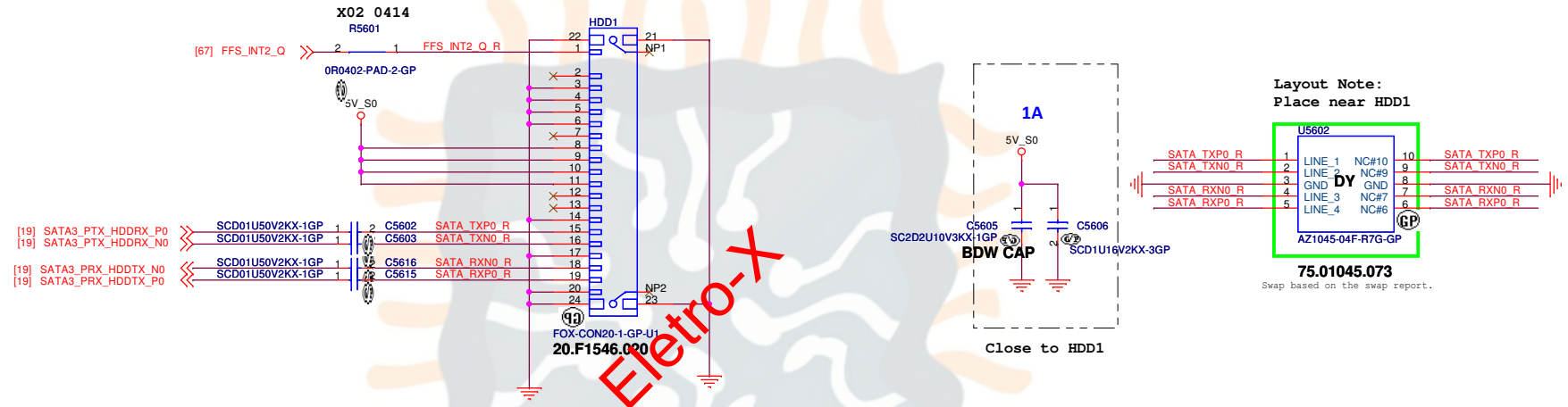
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Taipei Hsien 221, Taiwan, R.O.C.

Title **HDMI Level Shifter/Connector**
Size A3 Document Number
Date: Tuesday, June 17, 2014 Sheet 54

ELETRO-2

SSID = SATA

SATA HDD Connector



<Core Design>



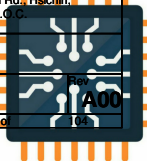
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **HDD/ODD**

Size A3 Document Number **Cottonwood**

Date: Tuesday, June 17, 2014

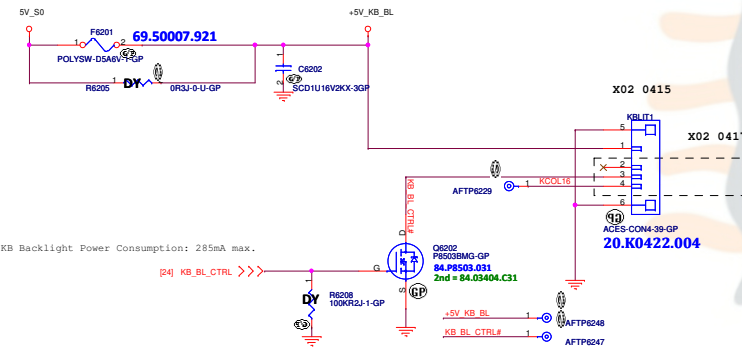
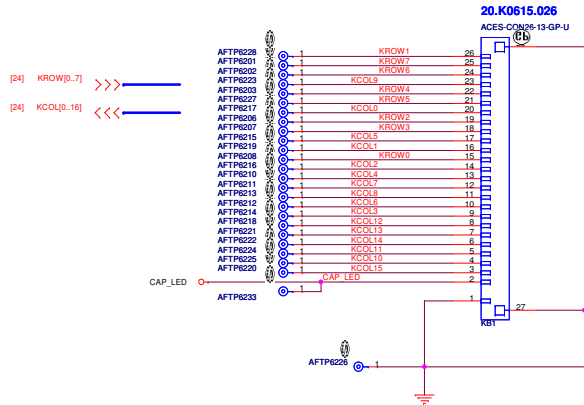
Sheet 56



ELECTRO-2

SSID = KBC

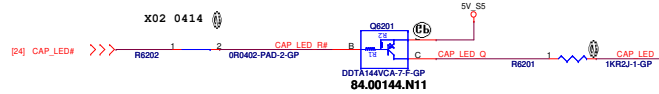
Keyboard



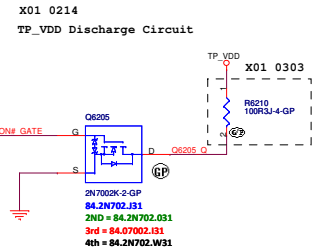
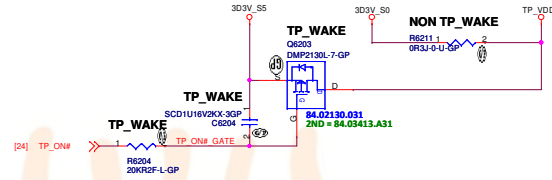
KB Backlight Power Consumption: 285mA max.

CAP LED Control

LOW active from KBC GPIO

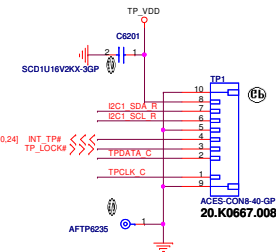


Touch.Pad

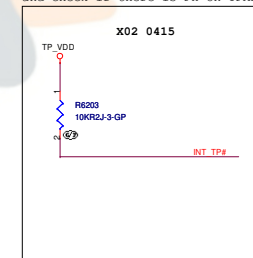


GPIO_TPADD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

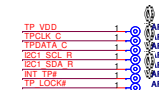
Touch Pad Connector



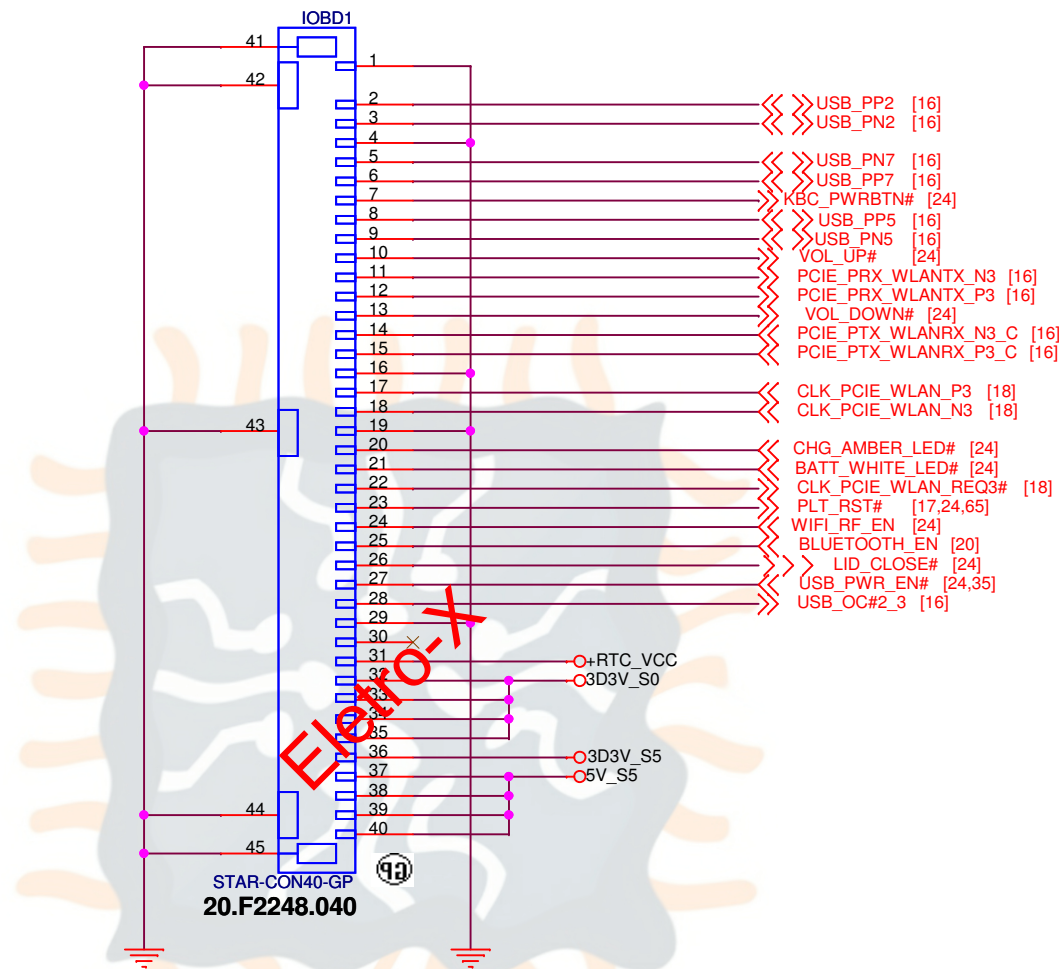
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



«Core Design»



<Core Design>



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Title

IO Board Connector

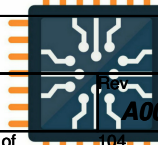
Size

Document Number

Cottonwood

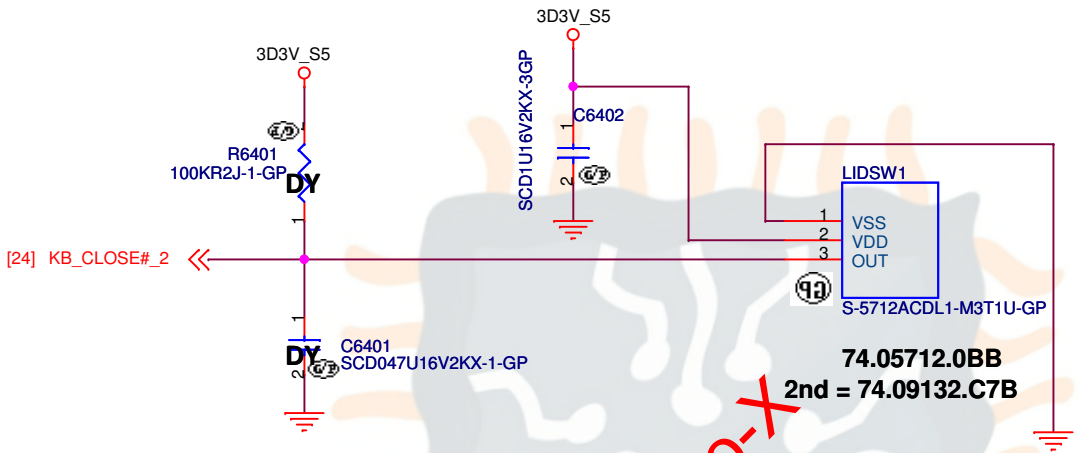
Date: Tuesday, June 17, 2014

Sheet 63 of 104



ELECTRO-X

SSID = User.Interface



<Core Design>

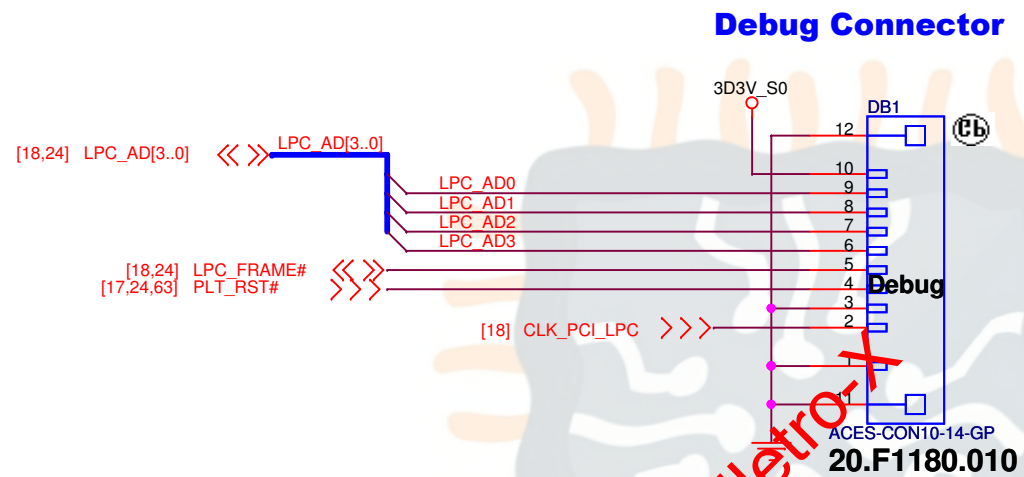


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Title		Hall Sensor	
Size	Document Number	Cottonwood	
A4		Rev A00	
Date:	Tuesday, June 17, 2014	Sheet	64 of 104

ELETRO-2

SSID = DEBUG PORT




20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41

DB1 Optional: New one smaller LPC connector is 20.F1180.010.

X01 0214



<Core Design>



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Title

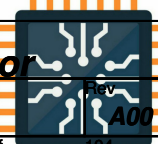
Dubug connector

Size
A4

Document Number
Cottonwood

Date: Tuesday, June 17, 2014

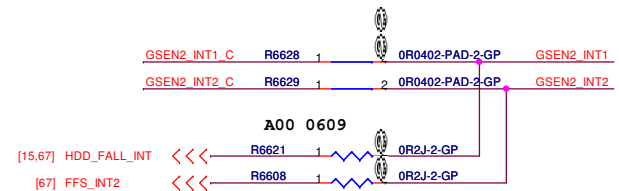
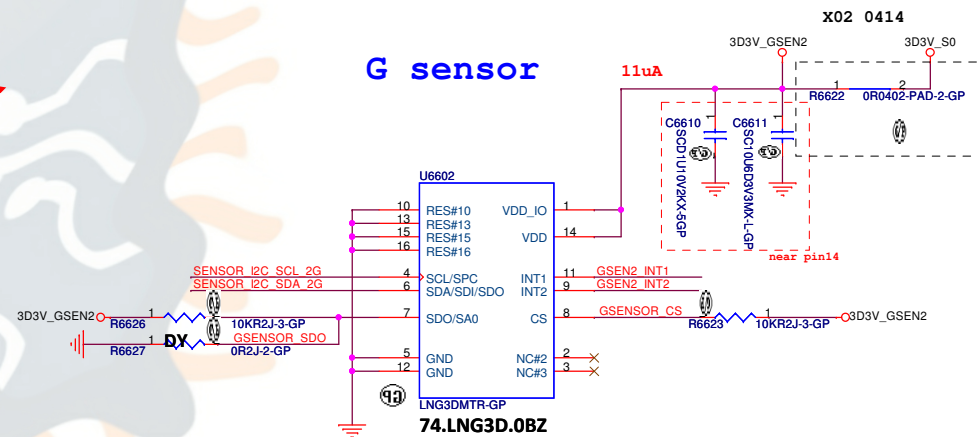
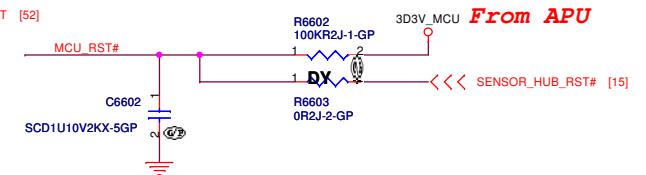
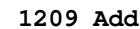
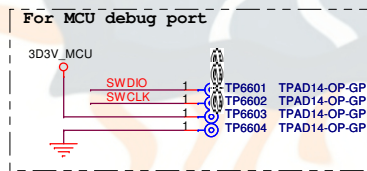
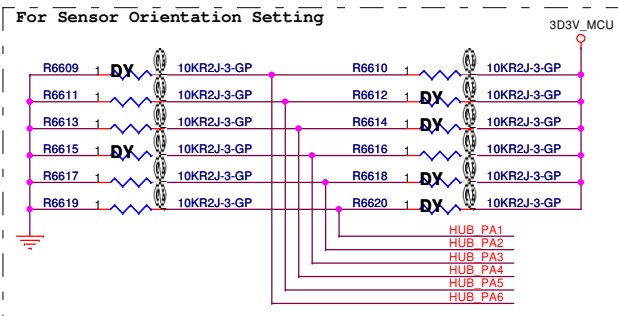
Sheet 65 of 104



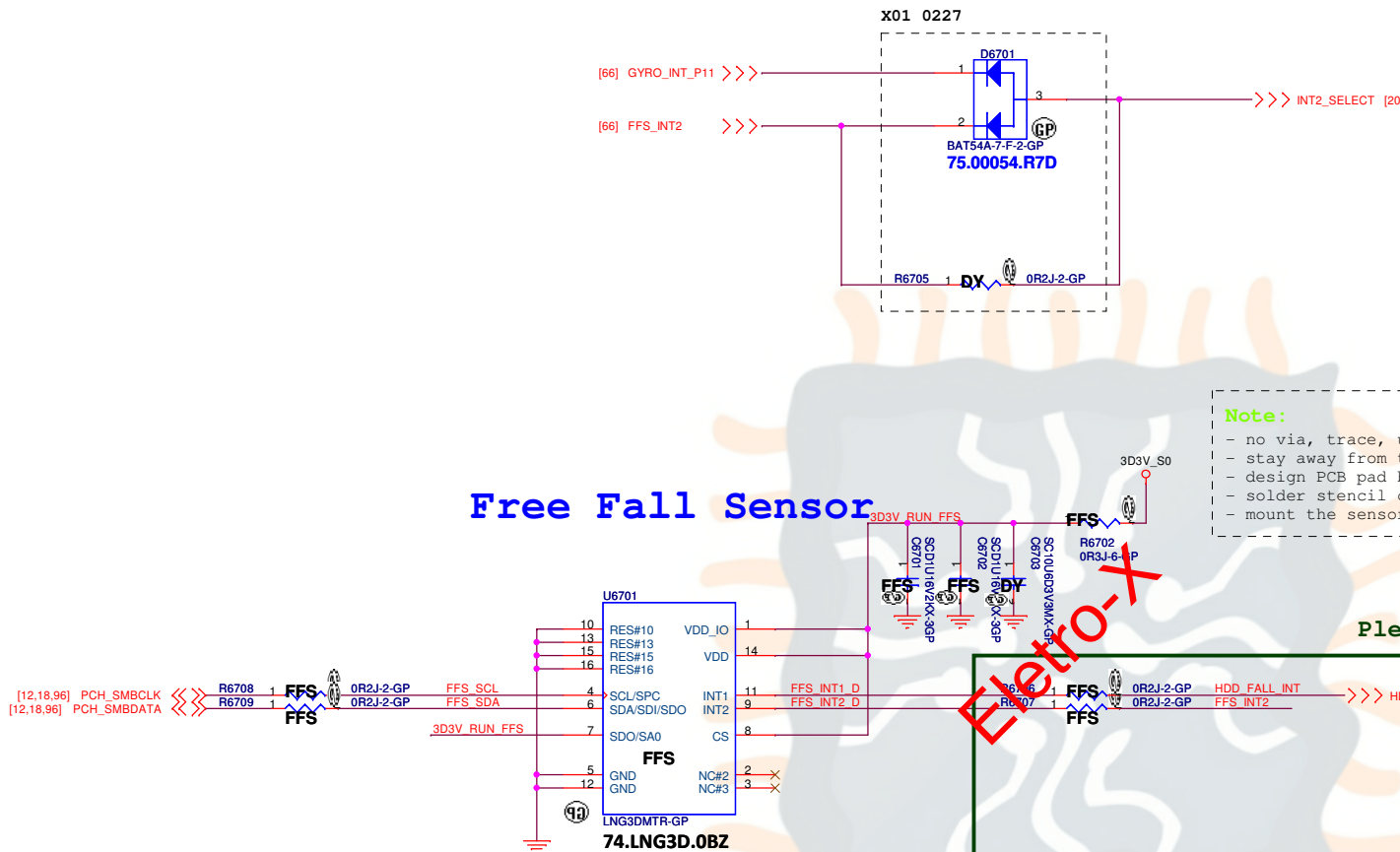
Rev
A00

ELECTRO-X

```
*Sensor HUB Version Differences
071.32151.000U is for Redwood
071.32151.0A0U is for Cottonwood
```



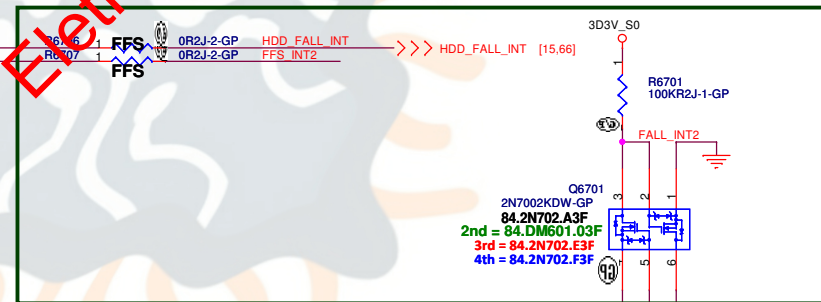
Free Fall Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

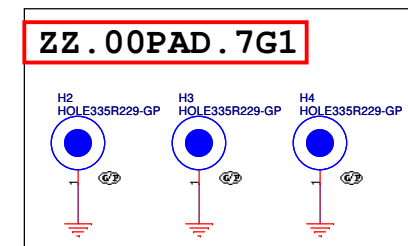
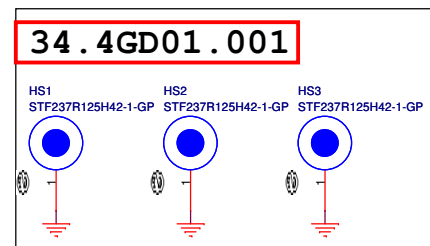
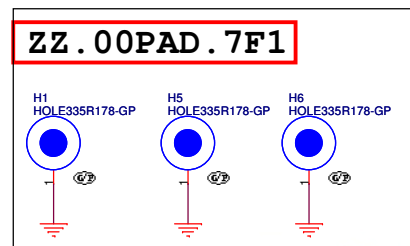
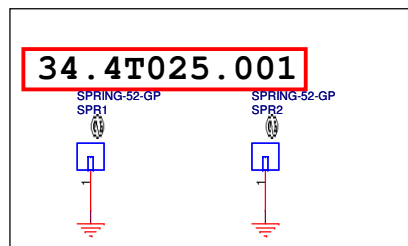
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Title	Reserved
Size A3	Document Number Cottonwood
Date: Tuesday, June 17, 2014	Sheet 67 of 103

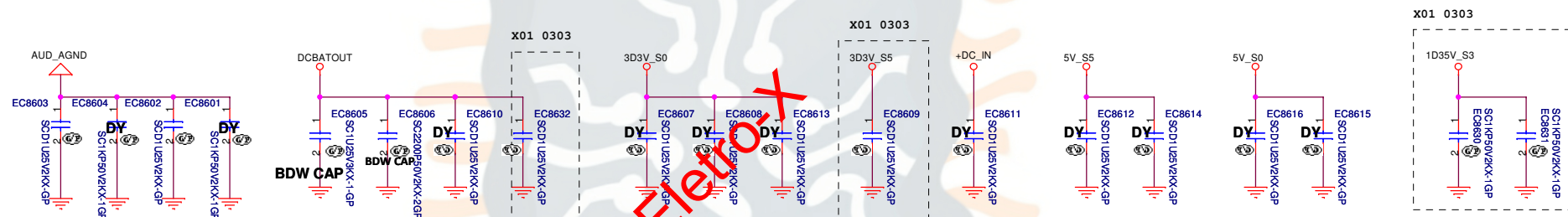
ELETRO-2

SSID = Mechanical

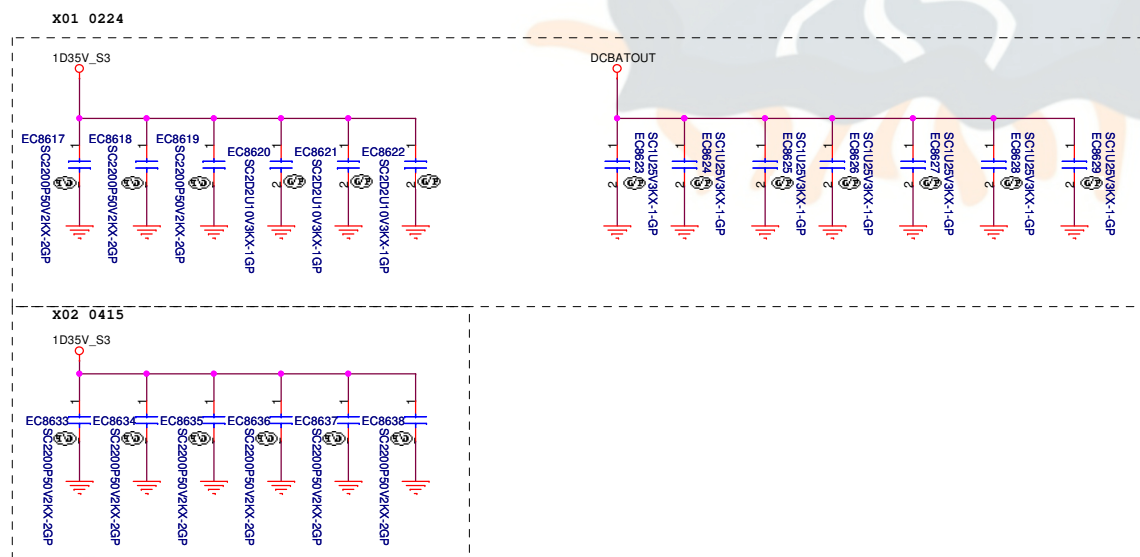


SSID = EMI

Mind the voltage rating of the caps.



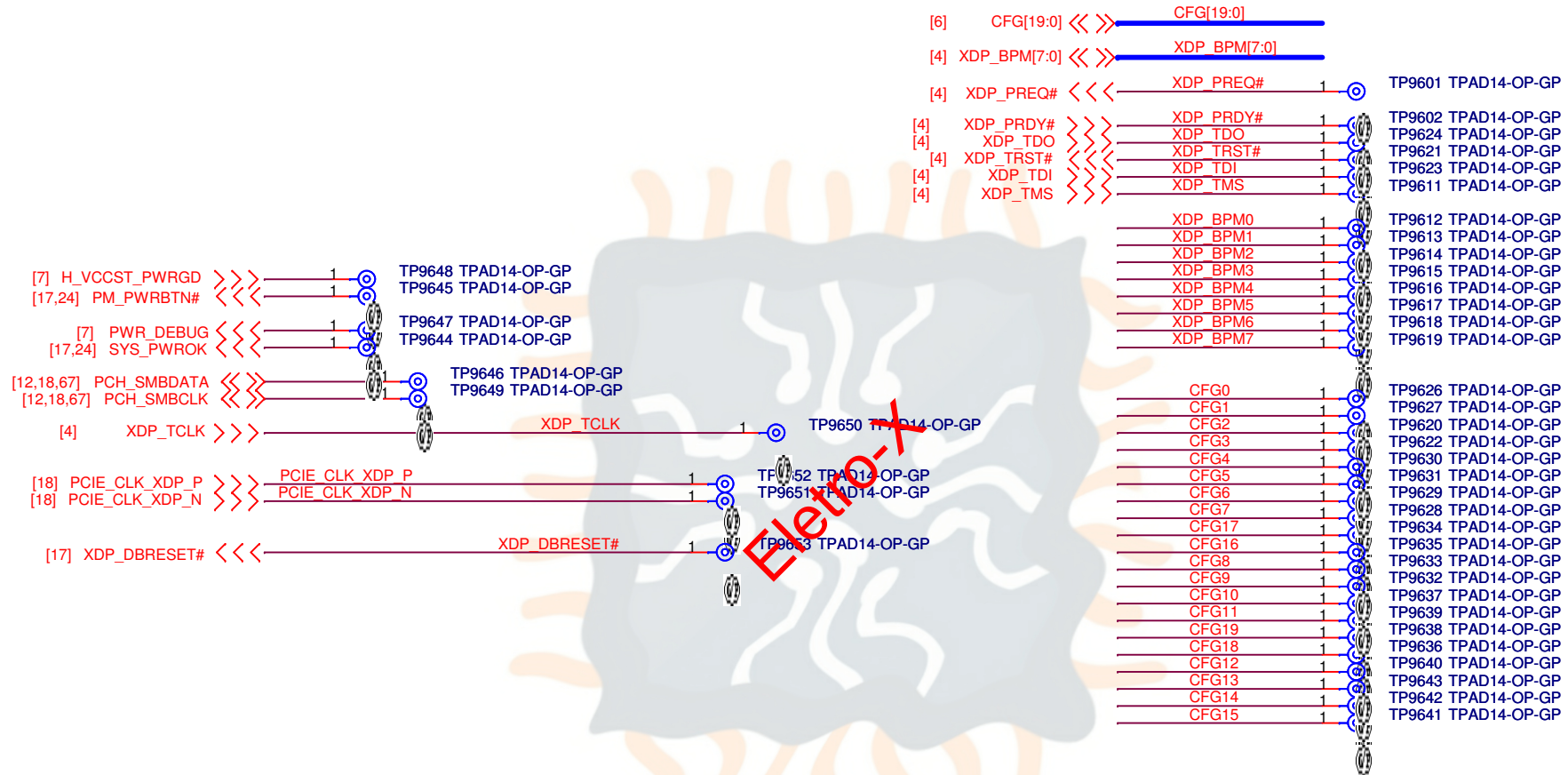
SSID = RF



<Core Design>

SSID = XDP

CPU XDP



<Core Design>



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Title

CPU/PCH XDP

Size

A4

Document Number

Cottonwood

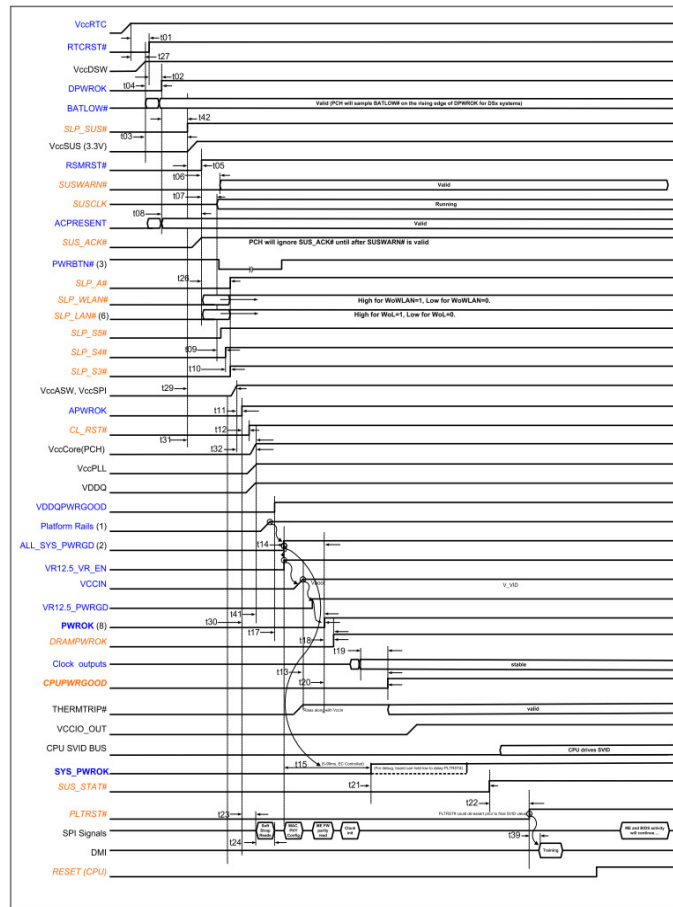
Date: Tuesday, June 17, 2014

Sheet 96 of 104

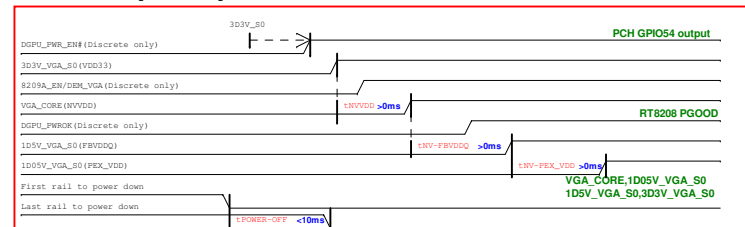


ELECTRO-2

Shark Bay Platform Power Sequence



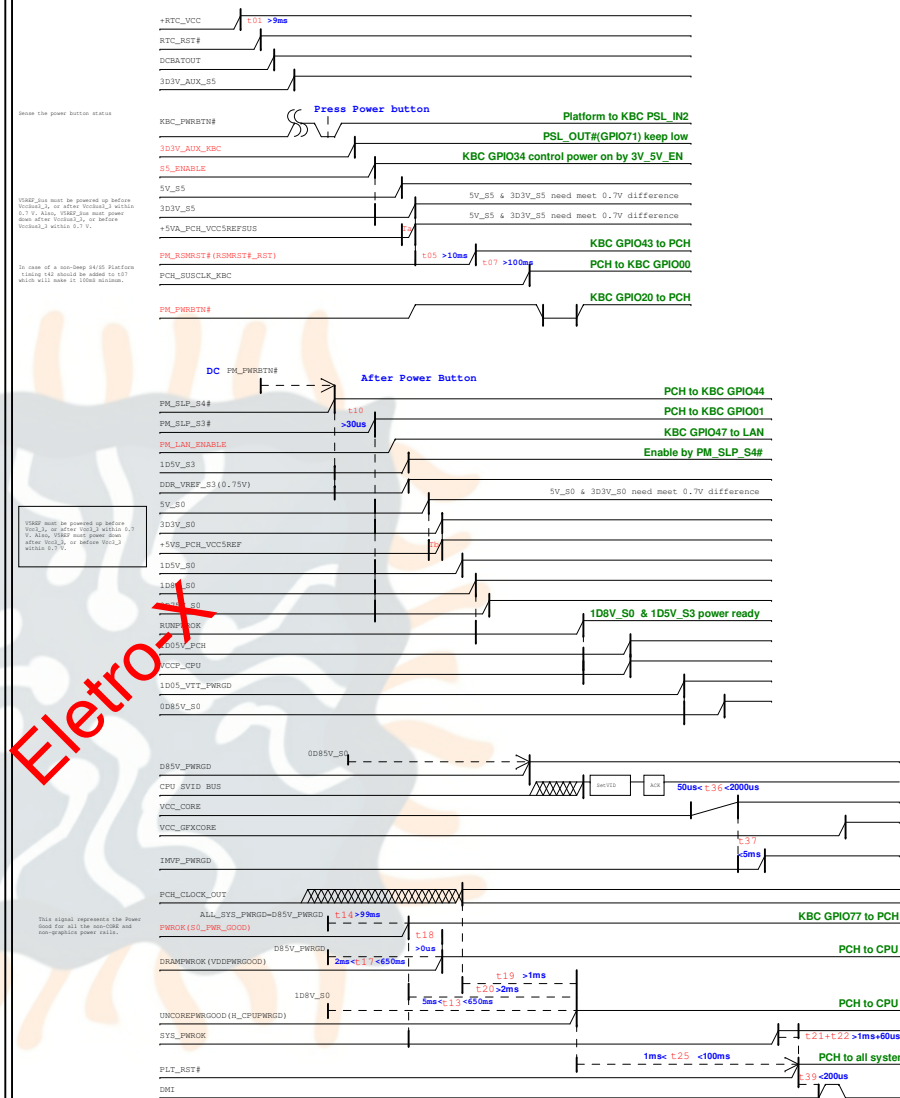
N14P-GT Power-Up/Down Sequence



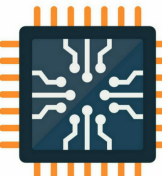
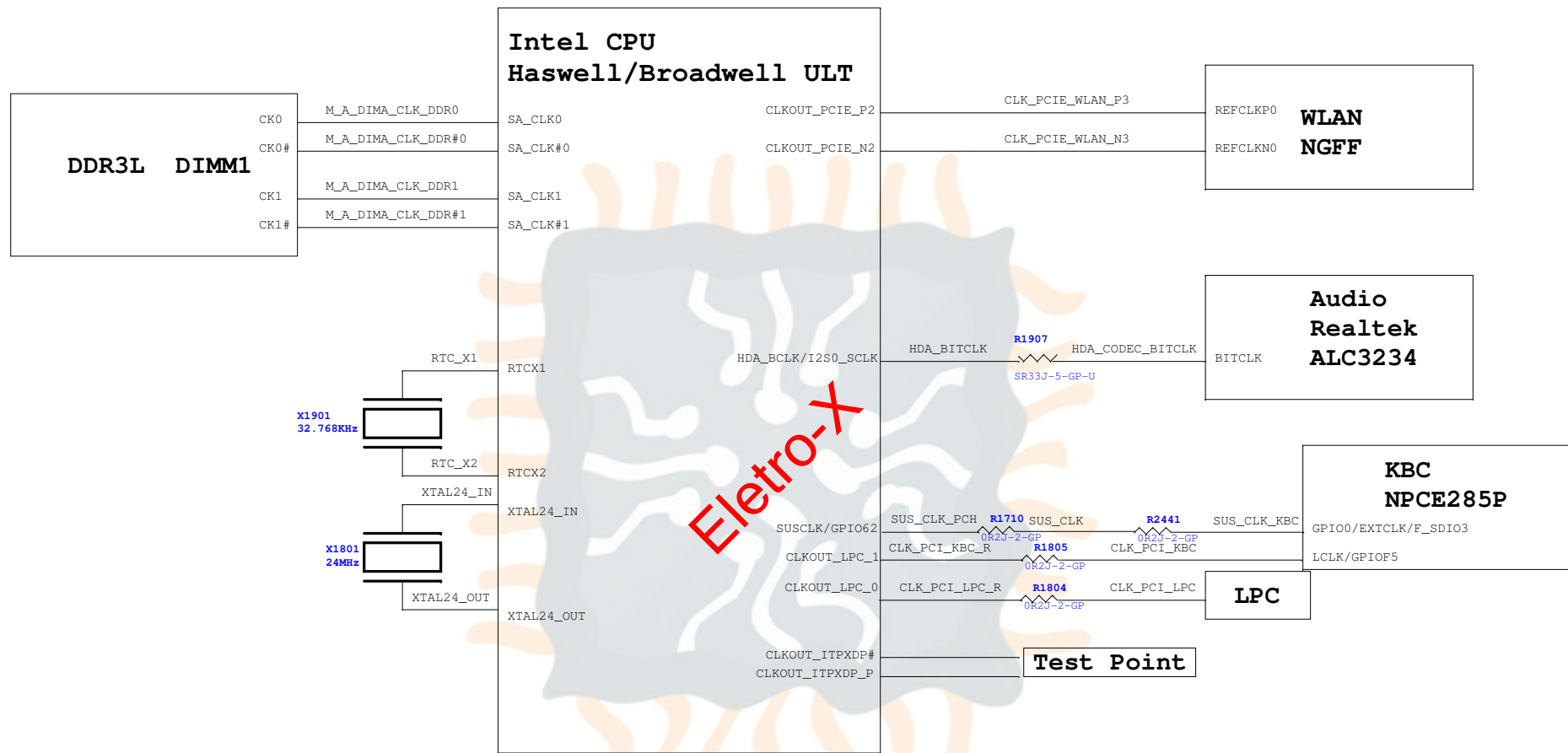
For power-down, reversing the ramp-up sequence is recommended.

(DC mode)


Red Words: Controlled by EC GPIO



CLK Block Diagram



[illegible][illegible][illegible]

Title		Change History		
Size	Document Number	Rev		
A3	Cottonwood	A00		
Date:	Tuesday, June 17, 2014	Sheet	103	104

